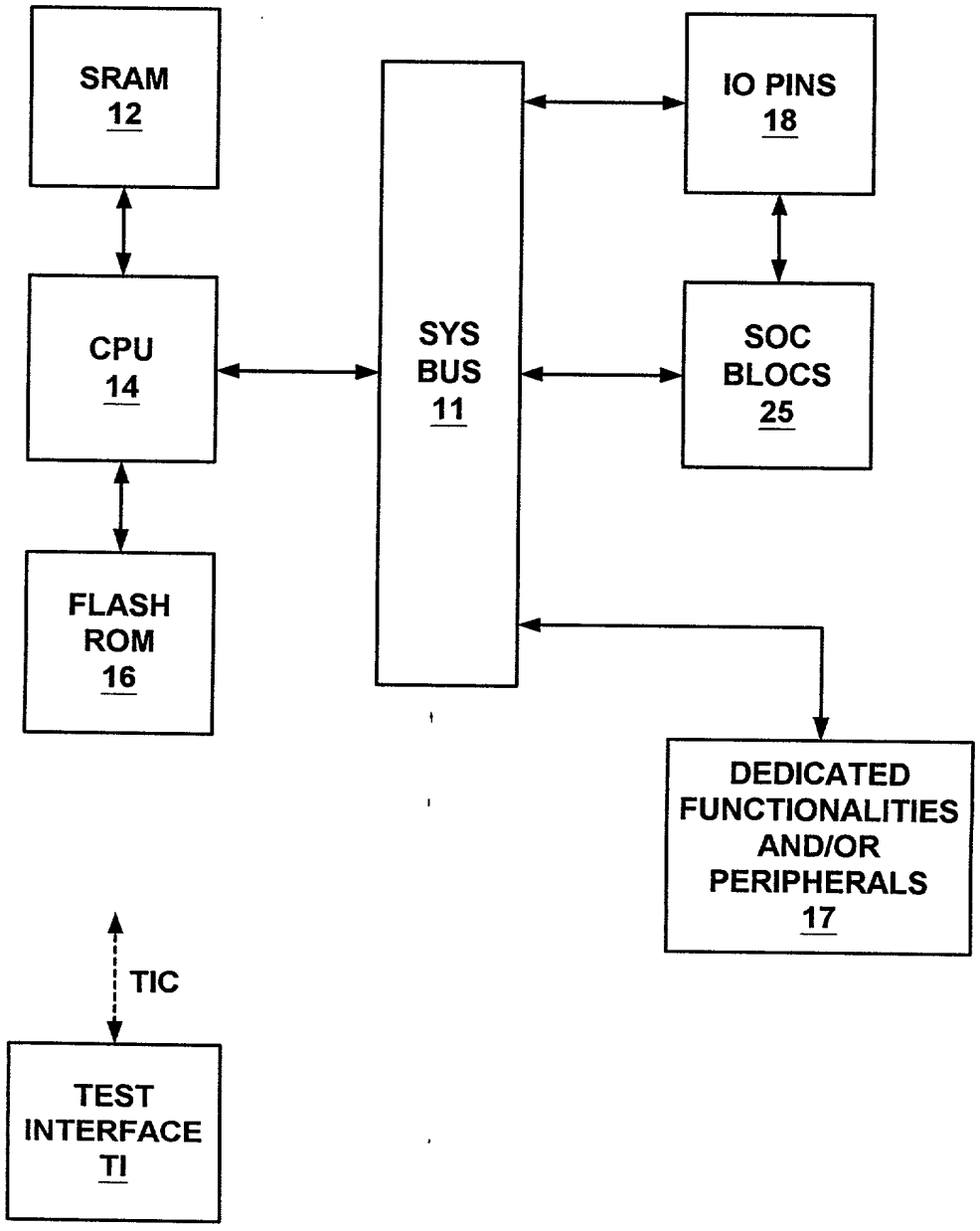
SRAM
12
IO PINS
18
CPU
14
SYS
BUS
11
SOC
BLOCS
25
FLASH
ROM
16
DEDICATED
FUNCTIONALITIES
AND/OR
PERIPHERALS
17
TIC
TEST
INTERFACE
TI

FIGURE 1A

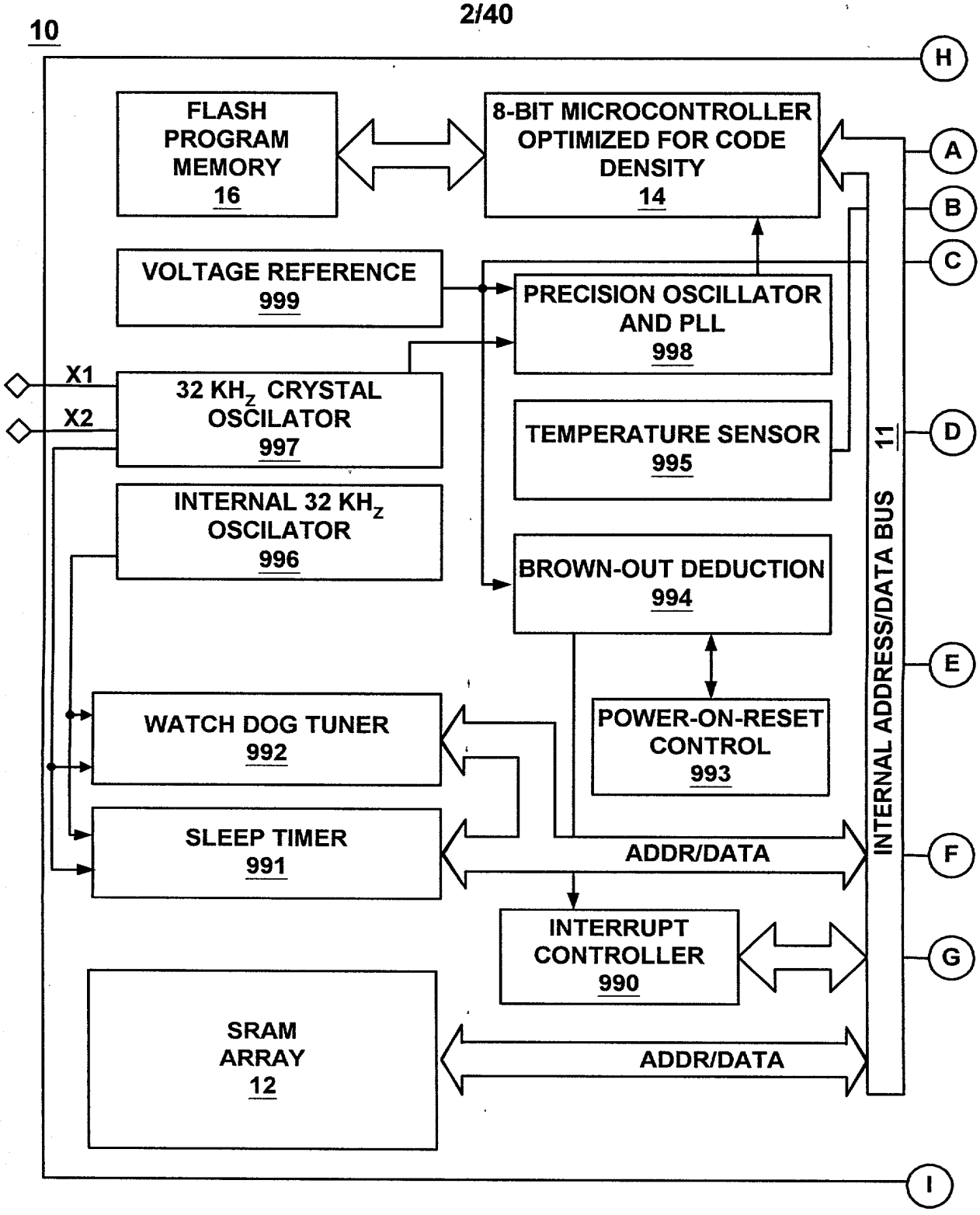
10
H
FLASH PROGRAM MEMORY 16
8-BIT MICROCONTROLLER OPTIMIZED FOR CODE DENSITY 14
A
B
C
VOLTAGE REFERENCE 999
PRECISION OSCILLATOR AND PLL 998
X1
X2
32 KHz CRYSTAL OSCILATOR 997
TEMPERATURE SENSOR 995
D
INTERNAL 32 KHz OSCILATOR 996
BROWN-OUT DEDUCTION 994
E
WATCH DOG TUNER 992
POWER-ON-RESET CONTROL 993
SLEEP TIMER 991
ADDR/DATA
F
INTERNAL ADDRESS/DATA BUS 11
INTERRUPT CONTROLLER 990
G
SRAM ARRAY 12
ADDR/DATA
I

FIGURE 1B

10 (CONT.)

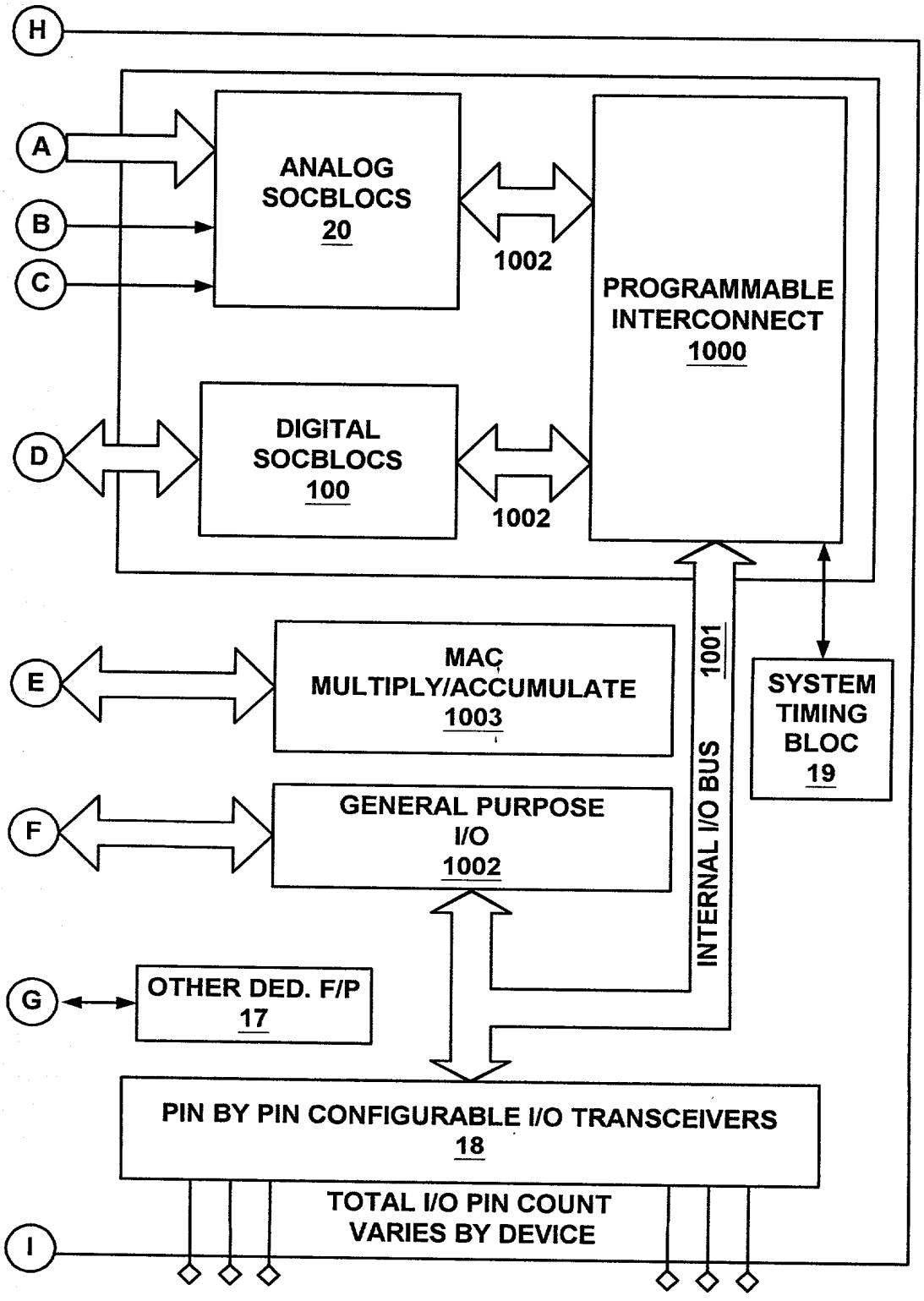

FIGURE 1B (CONT.)

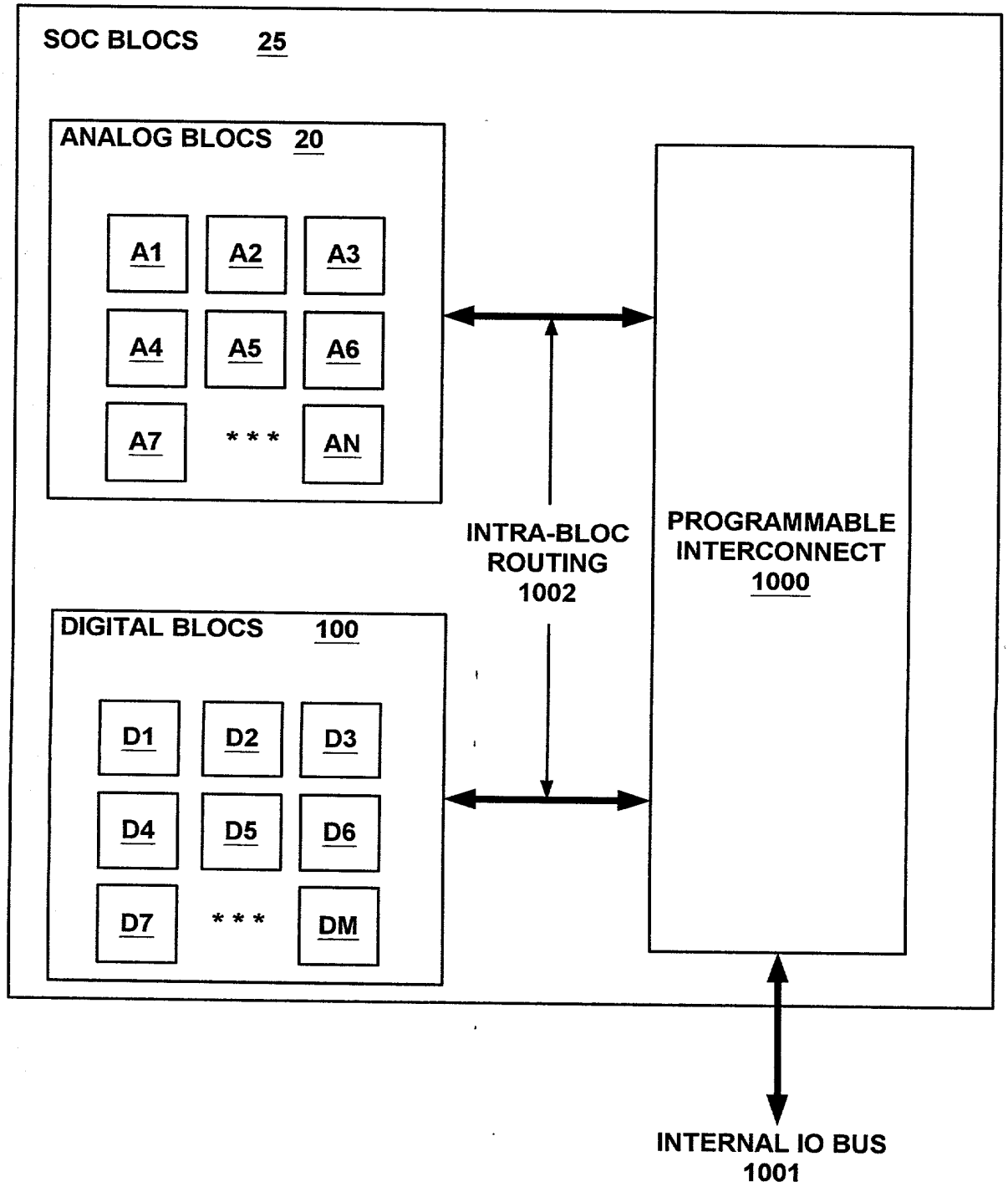
SOC BLOCS 25
ANALOG BLOCS 20
A1
A2
A3
A4
A5
A6
A7
* * *
AN
INTRA-BLOC ROUTING 1002
PROGRAMMABLE INTERCONNECT 1000
DIGITAL BLOCS 100
D1
D2
D3
D4
D5
D6
D7
* * *
DM
INTERNAL IO BUS 1001

FIGURE 1C

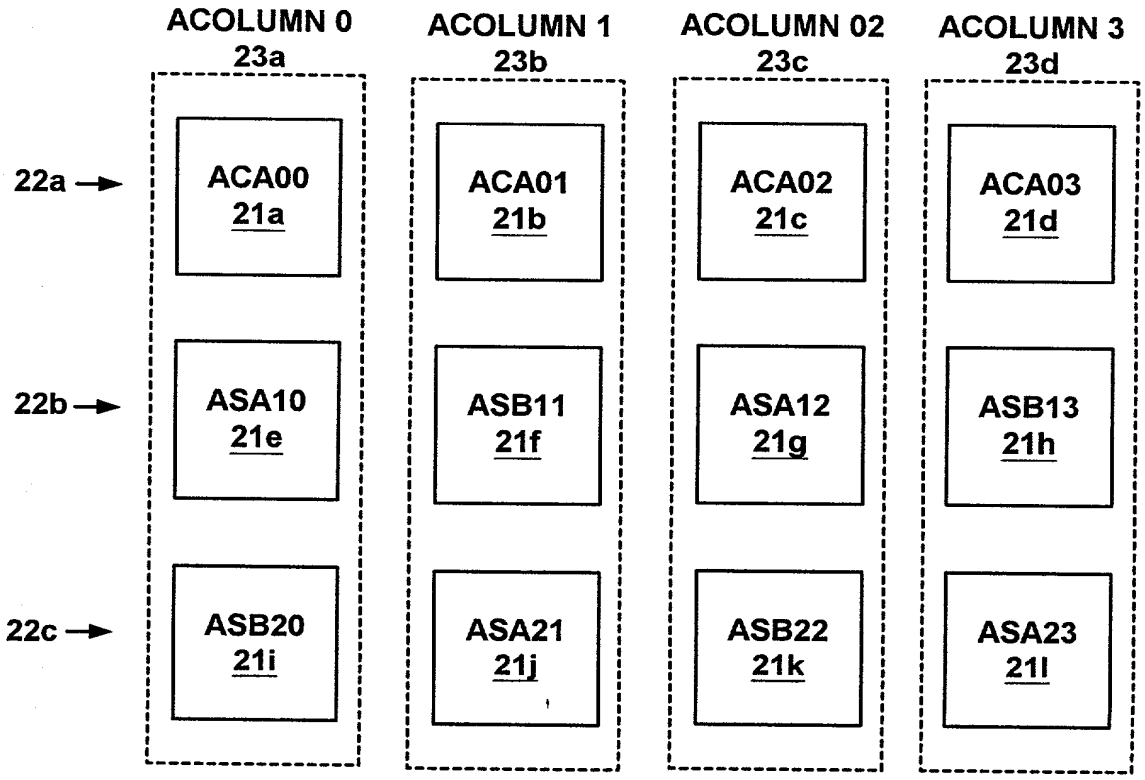
ACOLUMN 0
23a
ACOLUMN 1
23b
ACOLUMN 02
23c
ACOLUMN 3
23d
22a
22b
22c
ACA00
21a
ACA01
21b
ACA02
21c
ACA03
21d
ASA10
21e
ASB11
21f
ASA12
21g
ASB13
21h
ASB20
21i
ASA21
21j
ASB22
21k
ASA23
21l

FIGURE 2

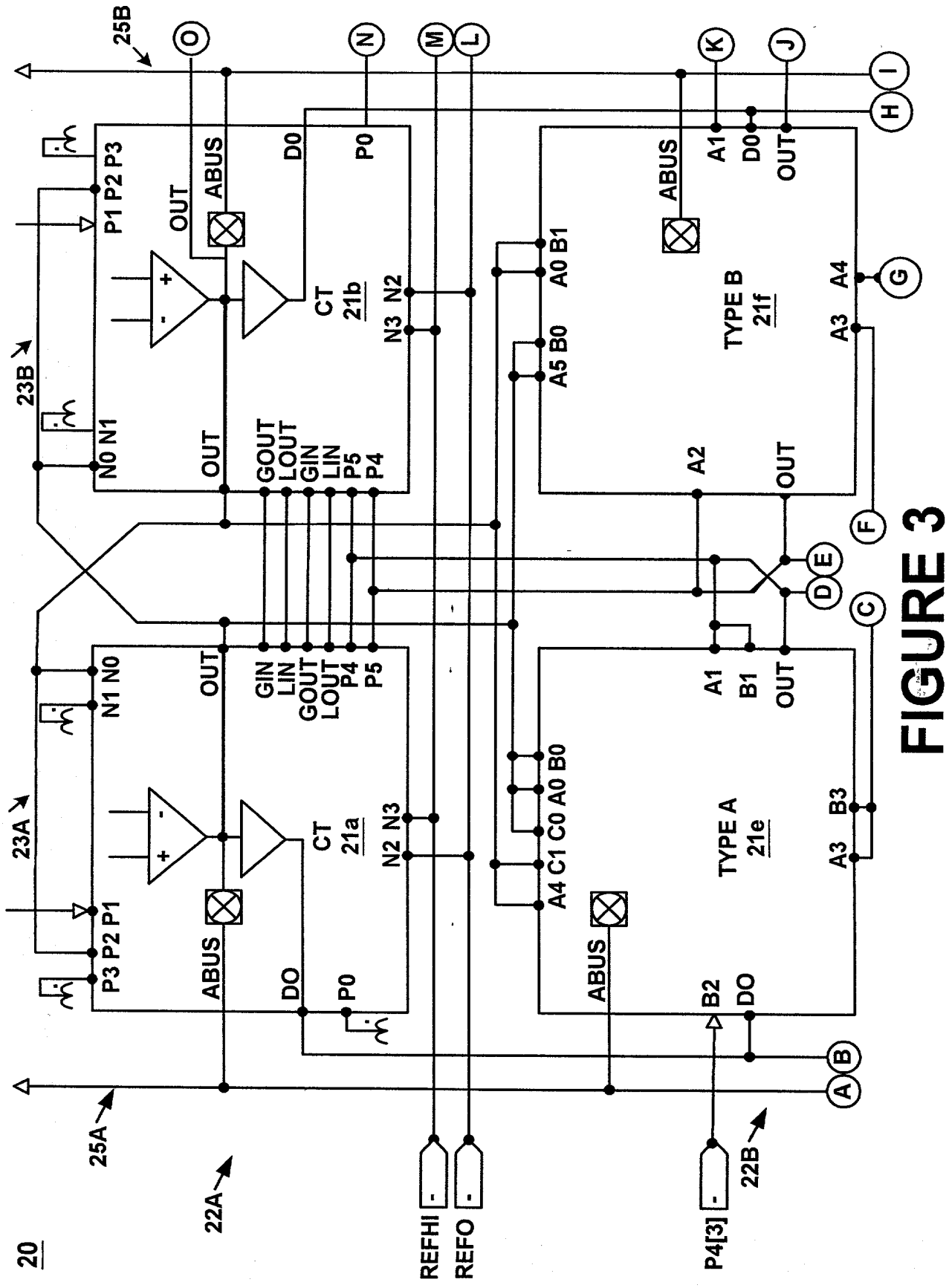
20
22A
22B
25A
25B
23A
23B
REFHI
REFO
P4[3]
CT
21a
21b
TYPE A
21e
TYPE B
21f
ABUS
OUT
DO
D0
P0
N0 N1
P1 P2 P3
N2 N3
GIN
LIN
GOUT
LOUT
P4
P5
A0 B1
A5 B0
A4 C1 C0 A0 B0
A1
B1
A2
A3 B3
A3 A4
B2
A1
D0
A
B
C
D
E
F
G
H
I
J
K
L
M
N
O

FIGURE 3

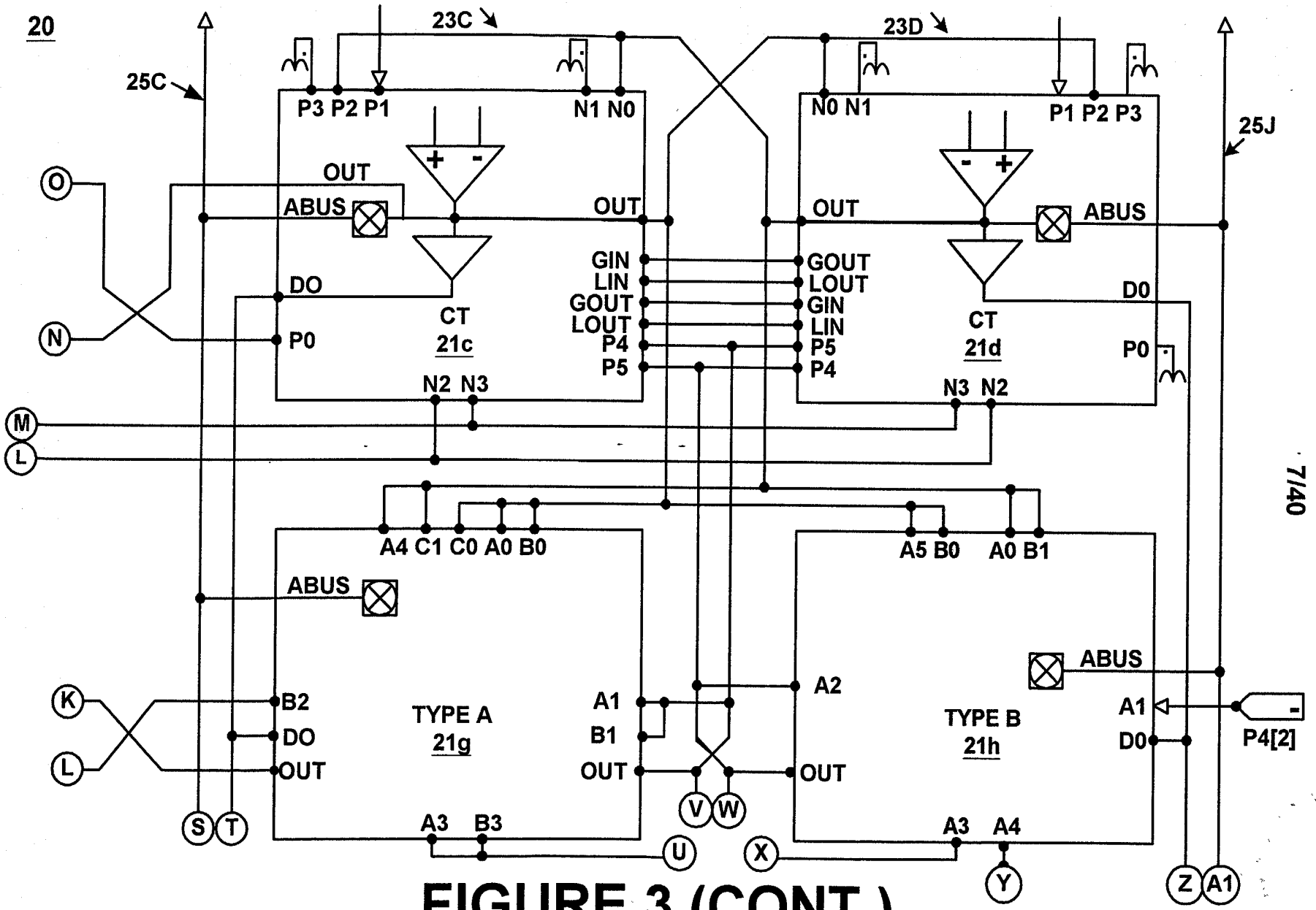

FIGURE 3 (CONT.)

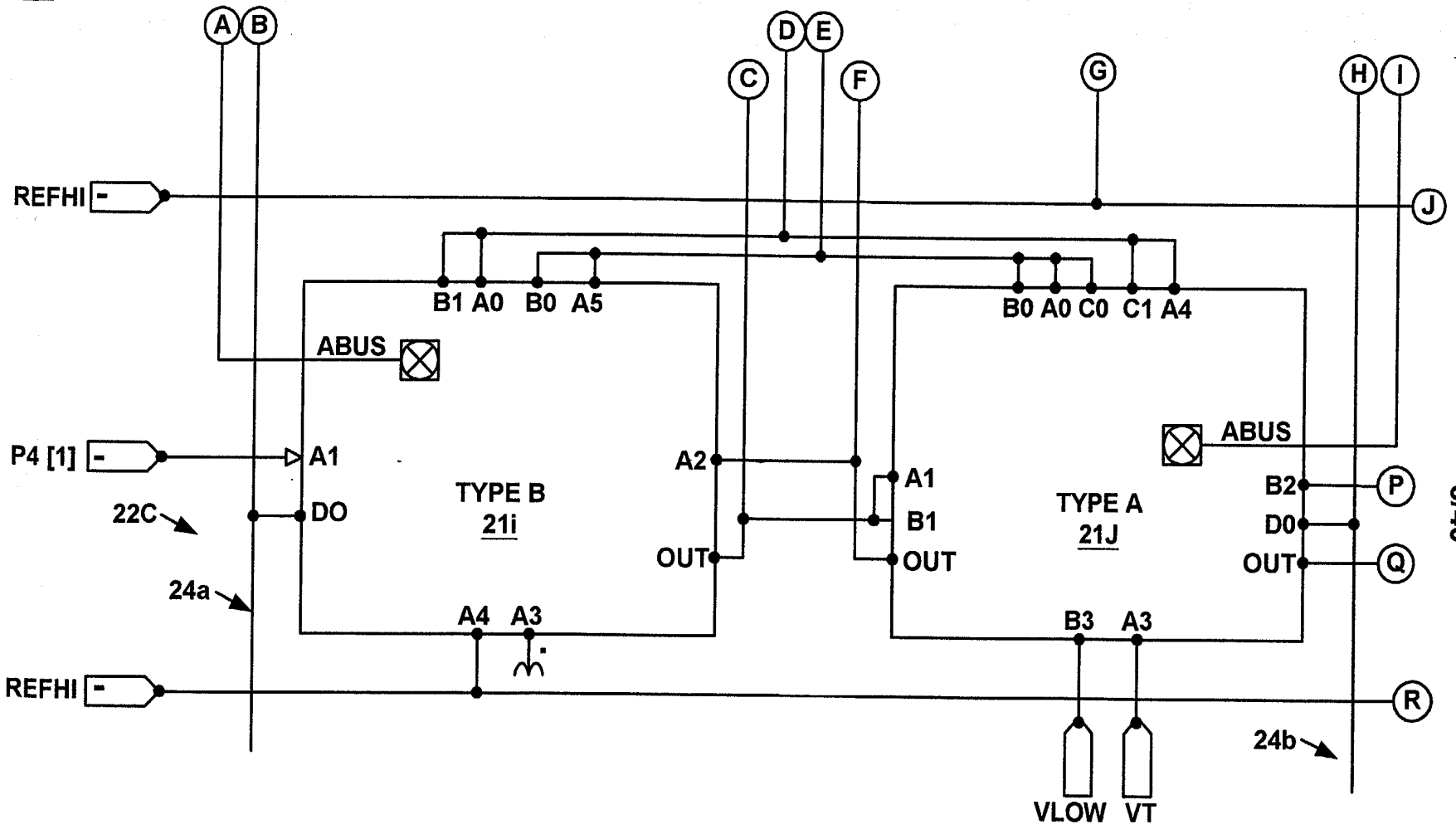

FIGURE 3 (CONT.)

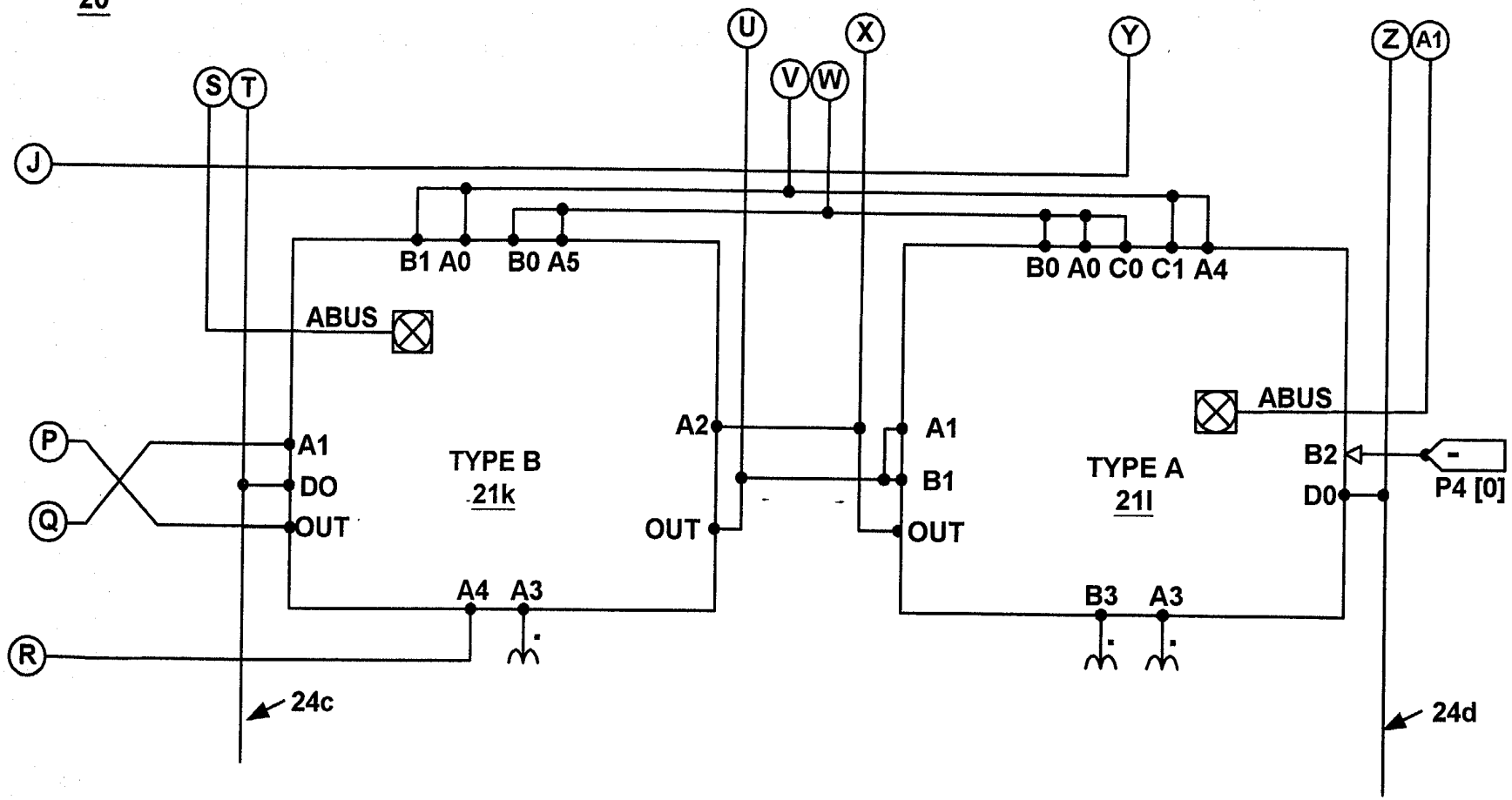

FIGURE 3 (CONT.)

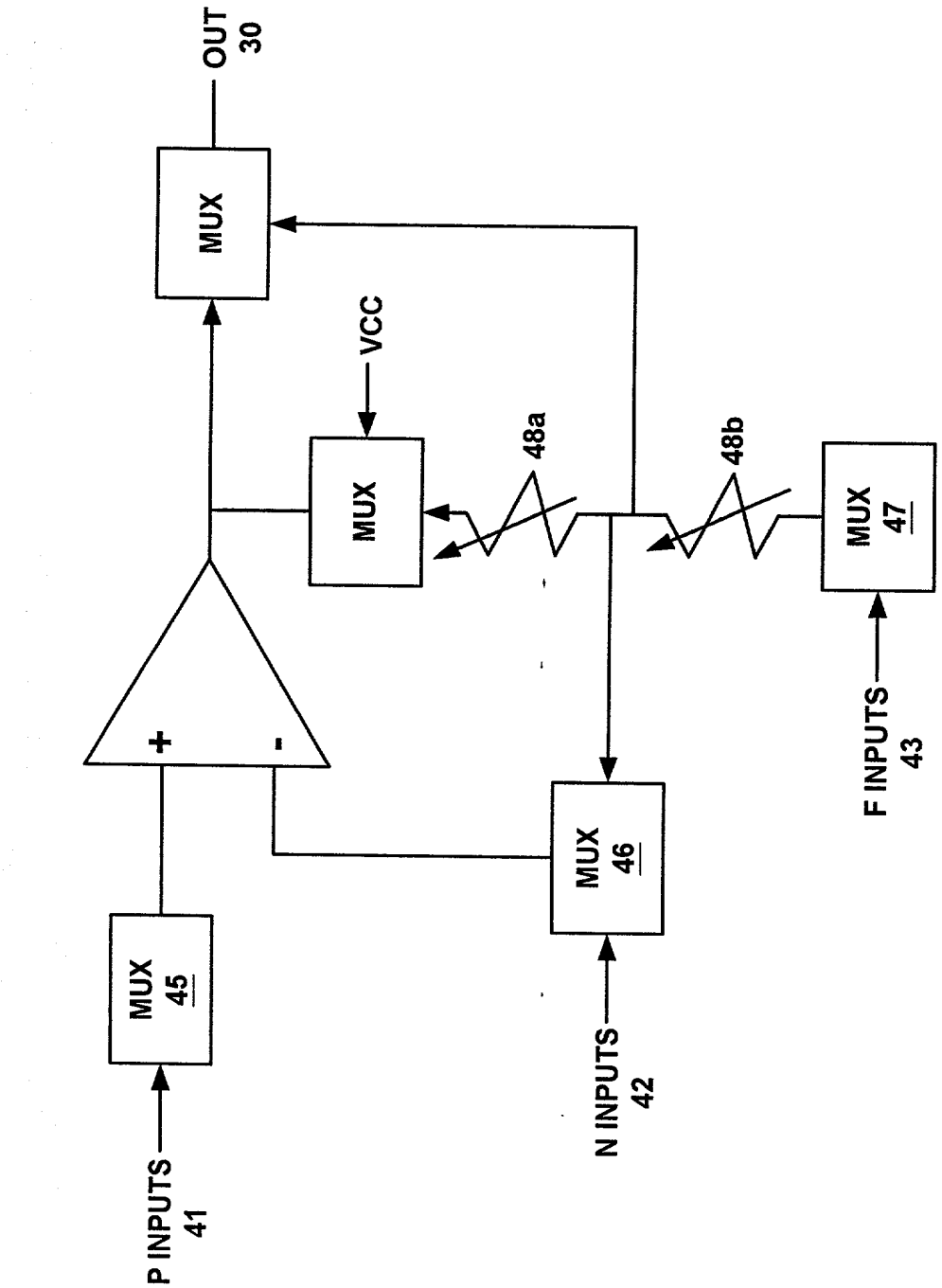
40
OUT
30
MUX
VCC
MUX
48a
48b
MUX
47
+
-
MUX
45
MUX
46
P INPUTS
41
N INPUTS
42
F INPUTS
43

FIGURE 4A

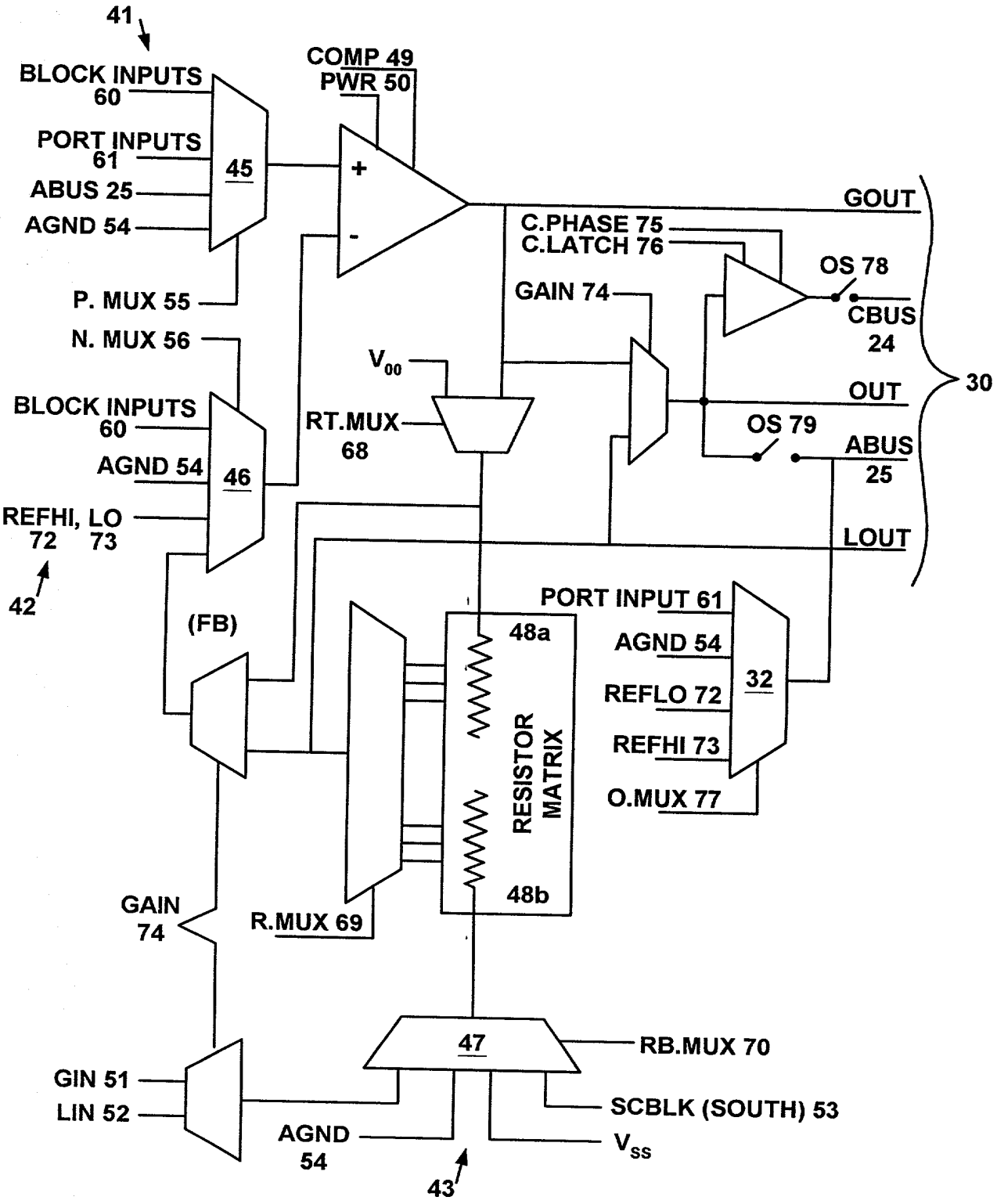
40
41
BLOCK INPUTS 60
PORT INPUTS 61
ABUS 25
AGND 54
45
P. MUX 55
N. MUX 56
COMP 49
PWR 50
+
-
GOUT
C.PHASE 75
C.LATCH 76
GAIN 74
OS 78
CBUS 24
OUT
OS 79
ABUS 25
LOUT
30
V_{00}
RT.MUX 68
BLOCK INPUTS 60
AGND 54
REFHI, LO 72 73
46
42
(FB)
48a
RESISTOR MATRIX
48b
PORT INPUT 61
AGND 54
REFLO 72
REFHI 73
O.MUX 77
32
GAIN 74
R.MUX 69
47
RB.MUX 70
GIN 51
LIN 52
AGND 54
SCBLK (SOUTH) 53
V_{SS}
43

FIGURE 4B

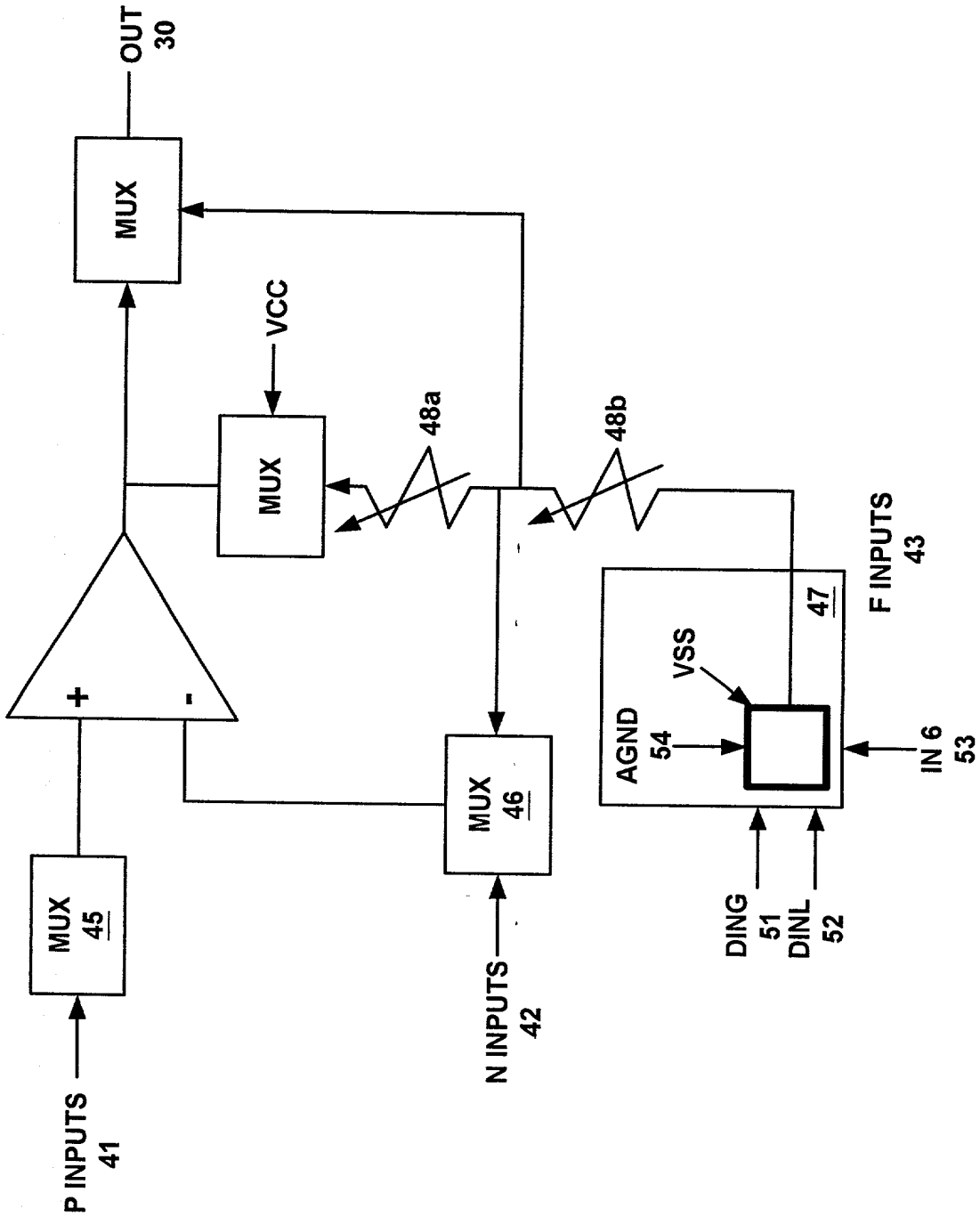
40
OUT
30
MUX
VCC
MUX
48a
48b
+
-
MUX
45
MUX
46
P INPUTS
41
N INPUTS
42
AGND
54
VSS
47
F INPUTS
43
IN 6
53
DING
51
DINL
52

FIGURE 5

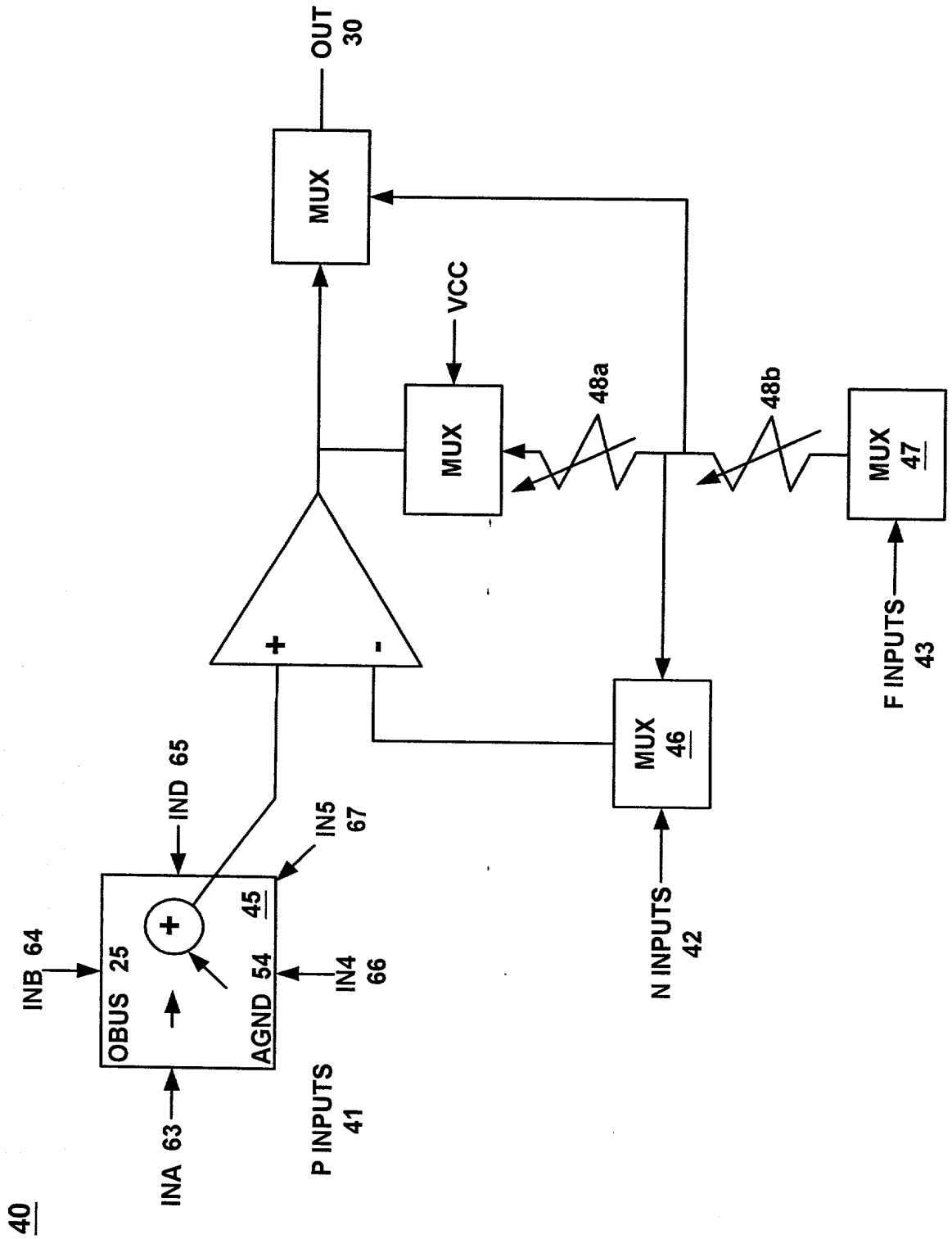
40
INA 63
INB 64
OBUS 25
AGND 54
45
P INPUTS 41
IND 65
IN5 67
IN4 66
N INPUTS 42
F INPUTS 43
MUX 46
MUX 47
MUX
VCC
48a
48b
OUT 30
+
-

FIGURE 6

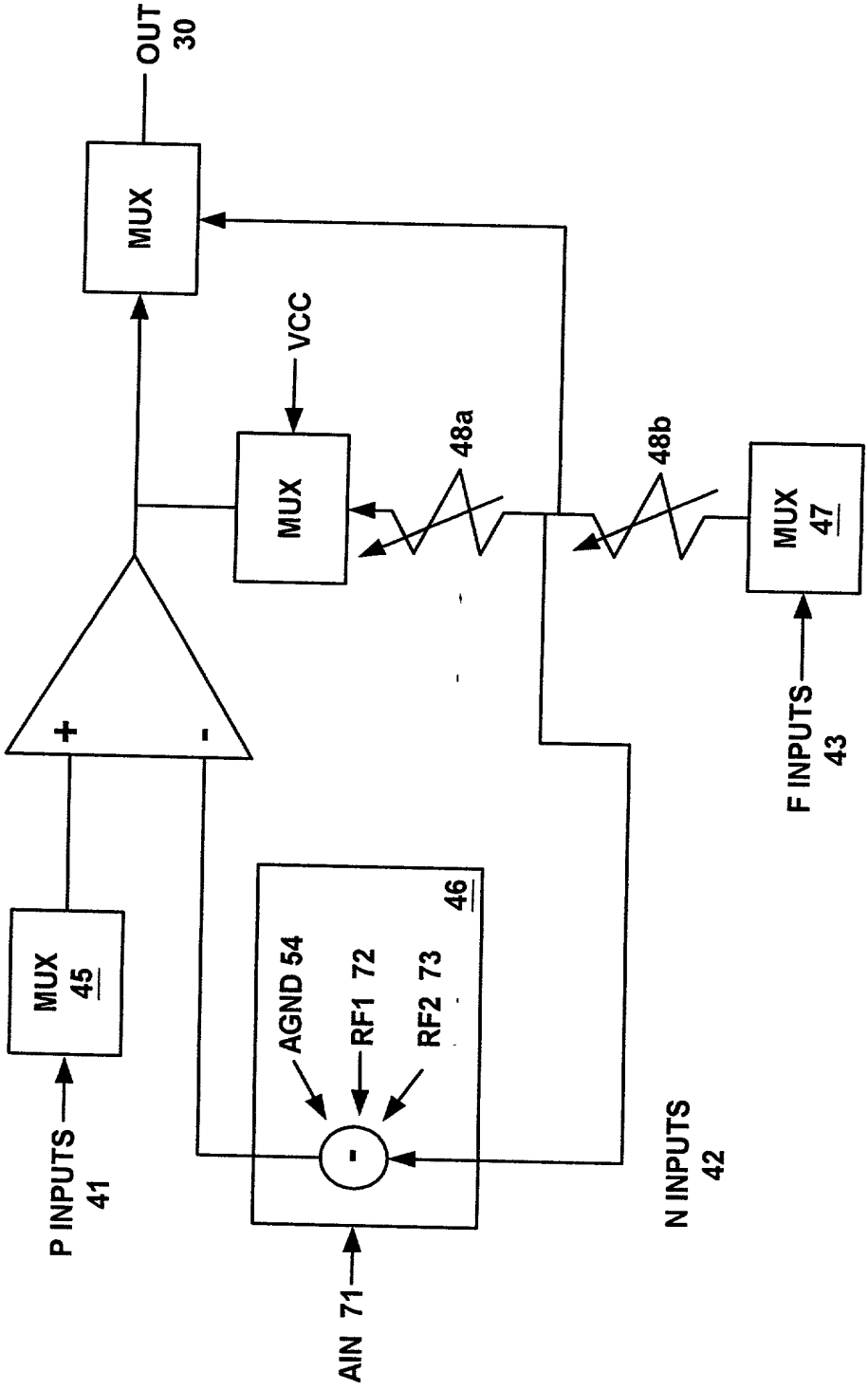
40
OUT
30
MUX
VCC
MUX
48a
48b
MUX
47
F INPUTS
43
+
-
MUX
45
P INPUTS
41
AGND 54
RF1 72
RF2 73
46
-
N INPUTS
42
AIN 71

FIGURE 7

80

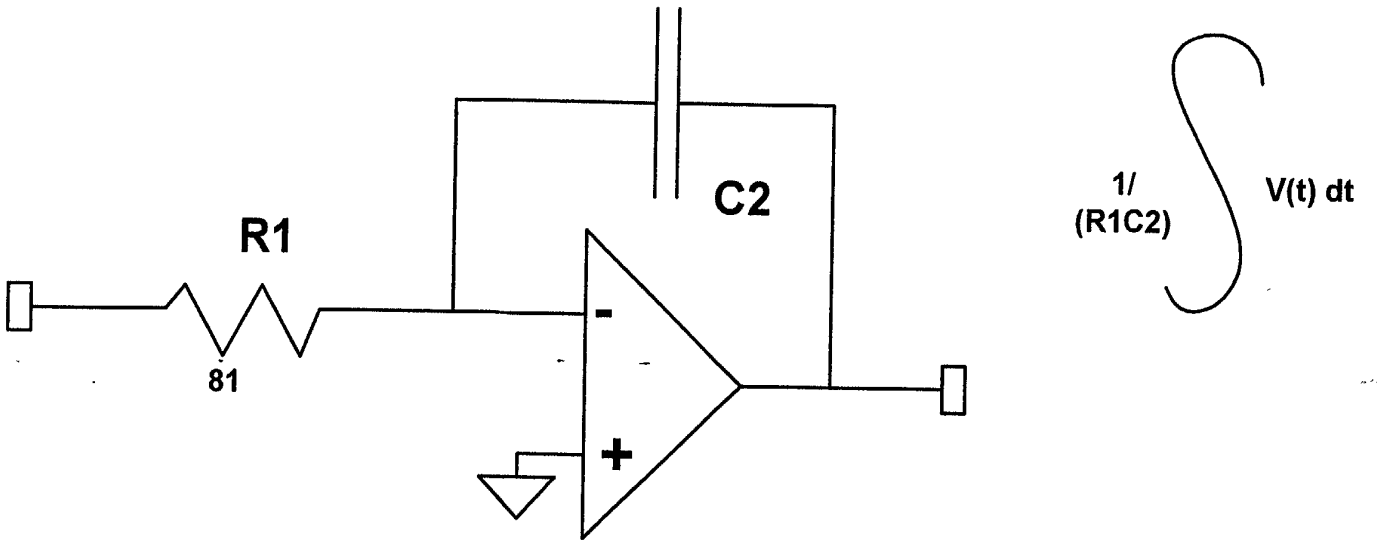

FIGURE 8A

85

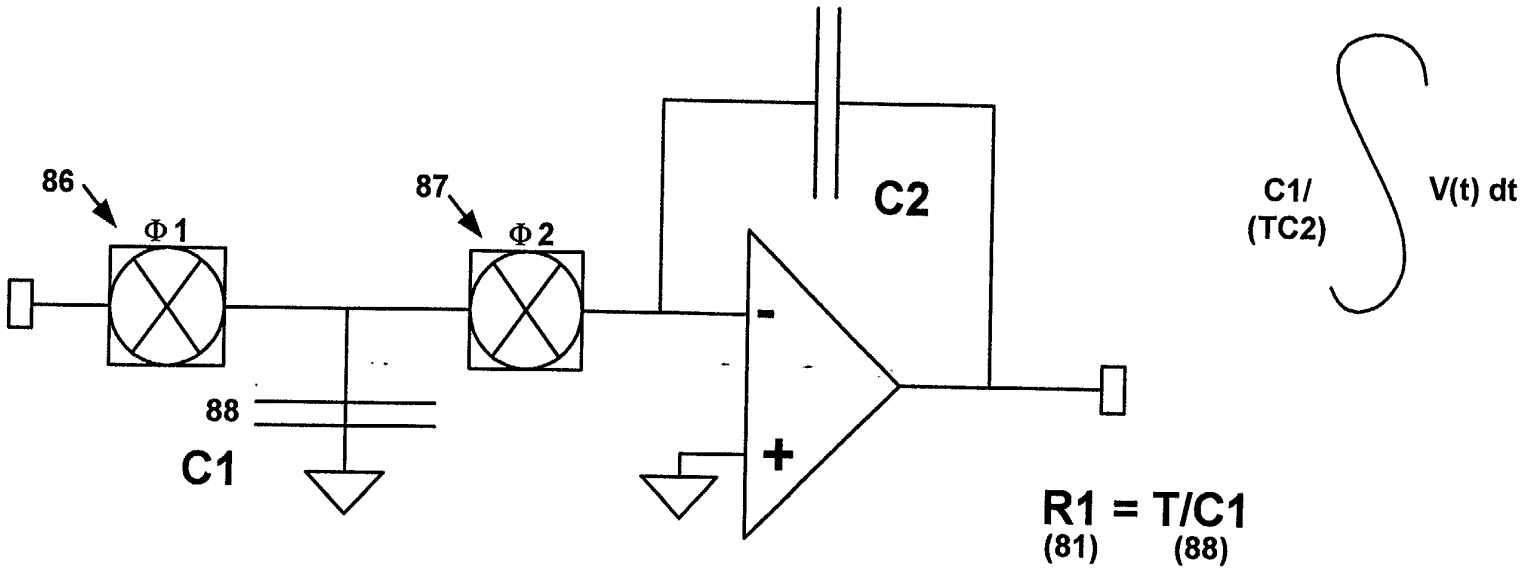

FIGURE 8B

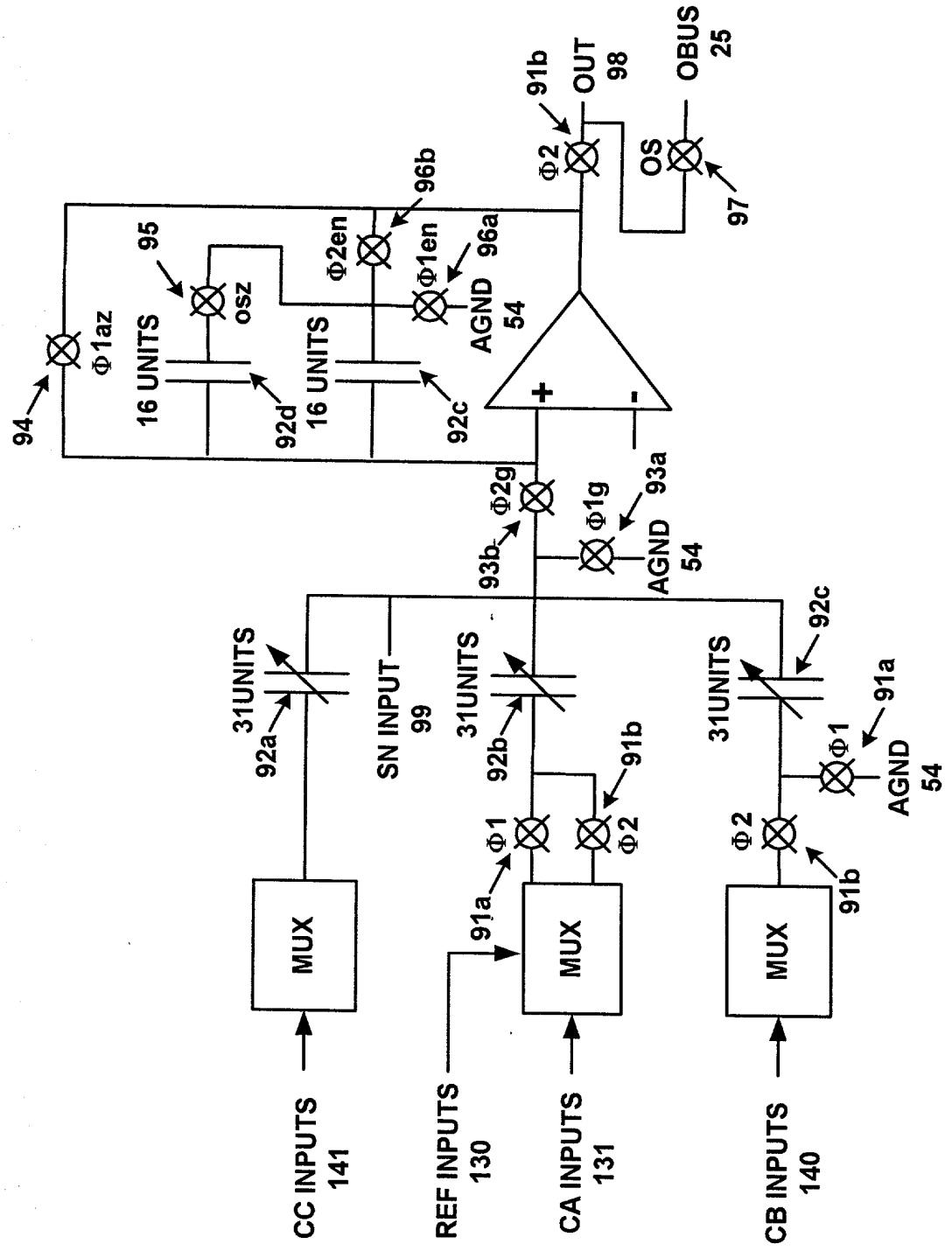
90
94
Φ1az
16 UNITS
95
osz
92d
16 UNITS
Φ2en
96b
Φ1en
96a
AGND
54
92c
+
-
Φ2
91b
OUT
98
OS
97
OBUS
25
Φ2g
93b
Φ1g
93a
AGND
54
31UNITS
92a
SN INPUT
99
31UNITS
92b
91b
Φ1
Φ2
91a
31UNITS
92c
91a
Φ1
AGND
54
Φ2
91b
MUX
MUX
MUX
CC INPUTS
141
REF INPUTS
130
CA INPUTS
131
CB INPUTS
140

FIGURE 9A

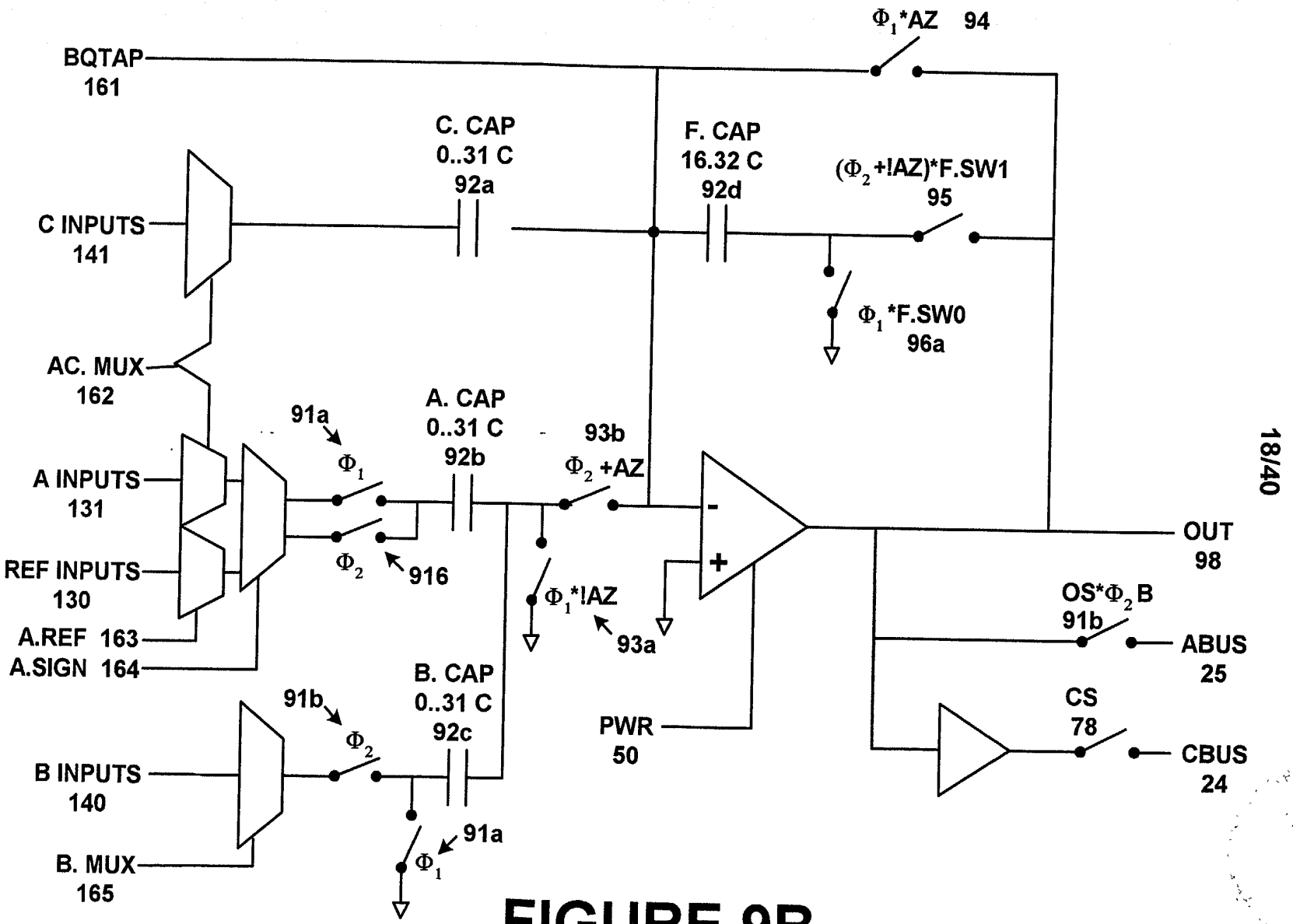
90a
BQTAP
161
Φ_1*AZ 94
C. CAP
0..31 C
92a
F. CAP
16.32 C
92d
(Φ_2+!AZ)*F.SW1
95
C INPUTS
141
Φ_1*F.SW0
96a
AC. MUX
162
91a
Φ_1
A. CAP
0..31 C
92b
93b
Φ_2 +AZ
A INPUTS
131
Φ_2
916
REF INPUTS
130
Φ_1*!AZ
93a
A.REF 163
A.SIGN 164
OUT
98
OS*Φ_2 B
91b
ABUS
25
B. CAP
0..31 C
92c
91b
Φ_2
PWR
50
CS
78
CBUS
24
B INPUTS
140
91a
Φ_1
B. MUX
165

FIGURE 9B

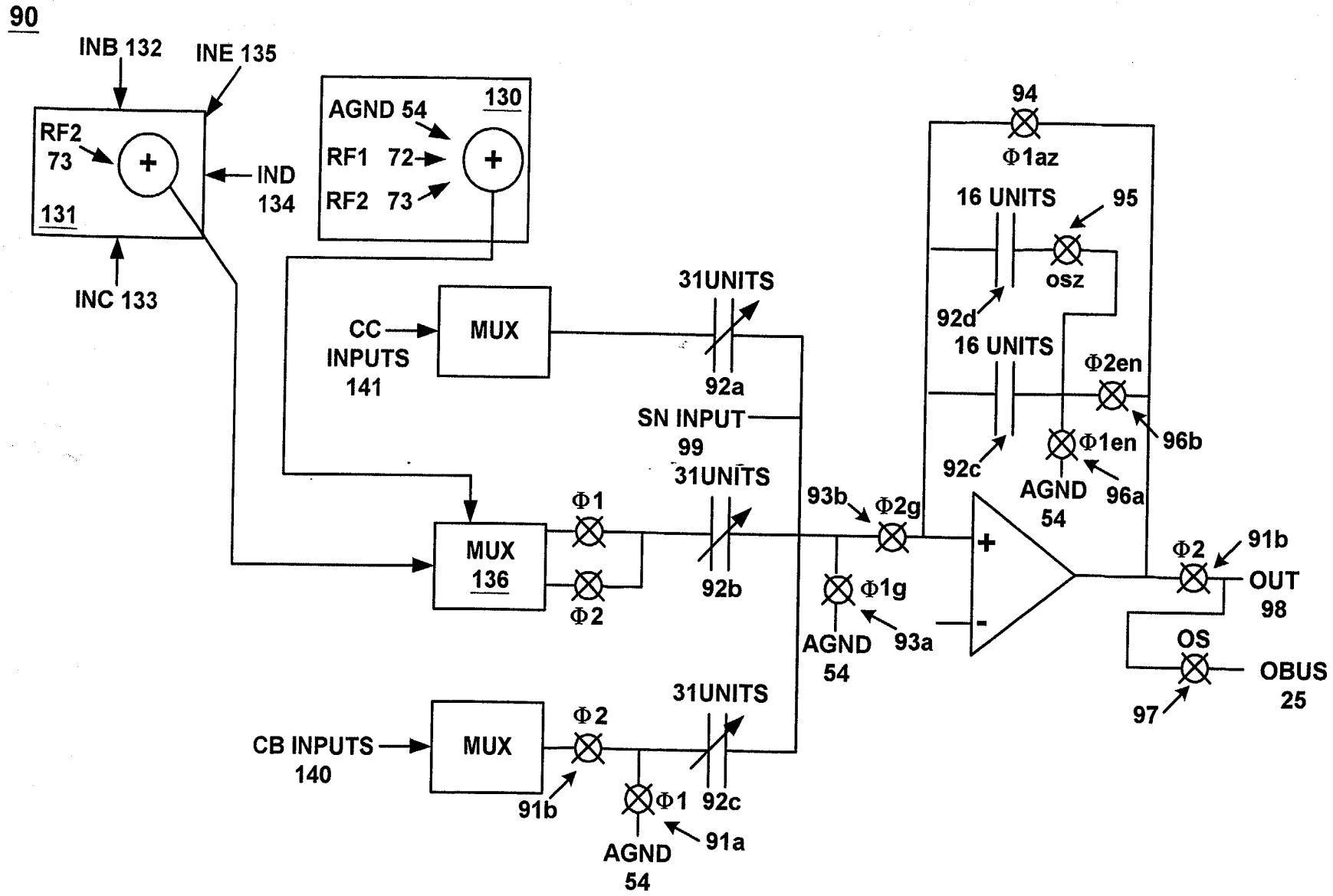
90
INB 132
INE 135
RF2
73
IND
134
131
INC 133
AGND 54
130
RF1 72
RF2 73
CC
INPUTS
141
MUX
31UNITS
92a
SN INPUT
99
MUX
136
Φ1
Φ2
31UNITS
92b
93b
Φ2g
Φ1g
AGND
54
93a
94
Φ1az
16 UNITS
95
osz
92d
16 UNITS
Φ2en
92c
Φ1en
96b
AGND
54
96a
Φ2
91b
OUT
98
OS
OBUS
25
97
CB INPUTS
140
MUX
Φ2
31UNITS
91b
Φ1
92c
AGND
54
91a

FIGURE 10

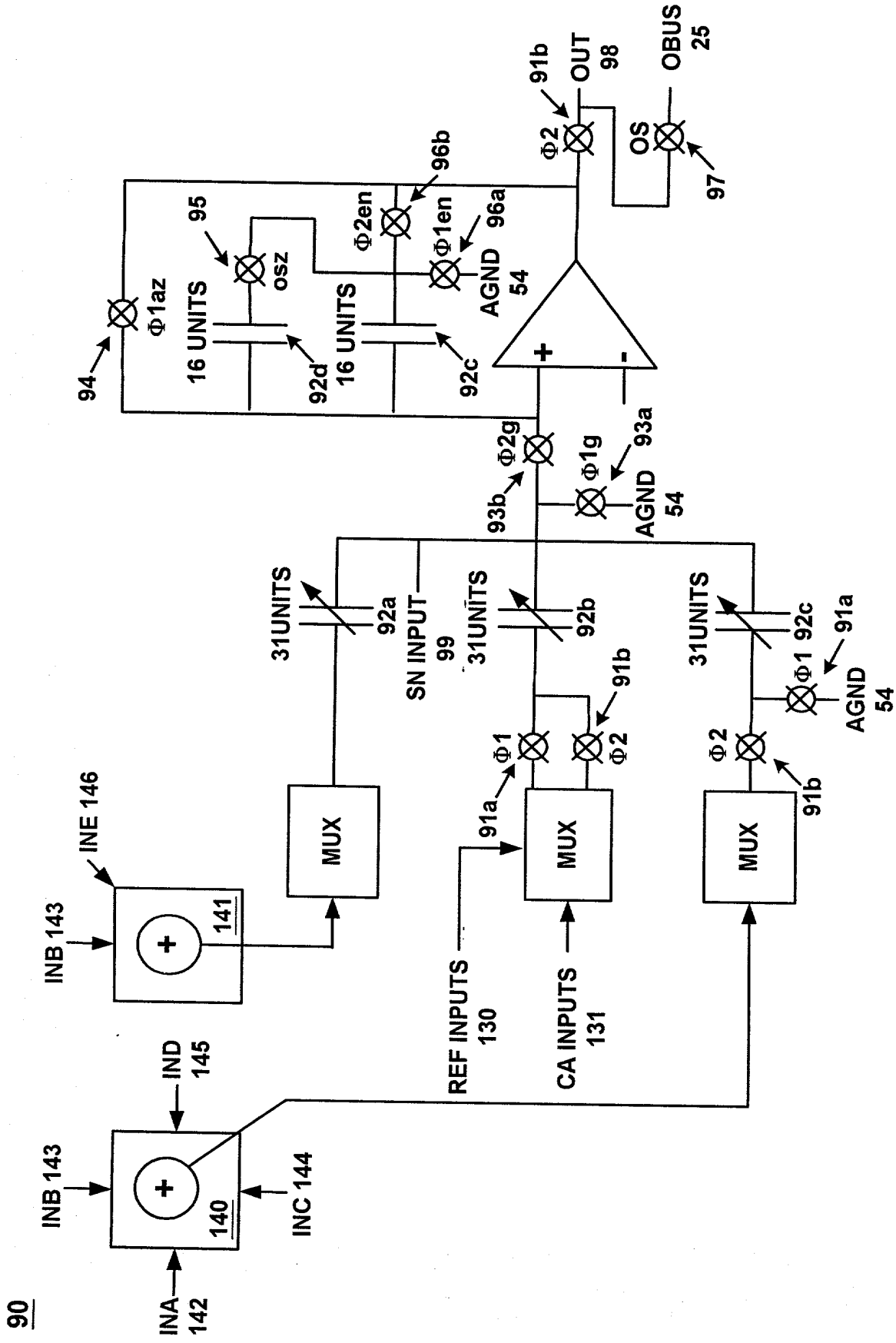
90
INA 142
INB 143
140
INC 144
IND 145
INB 143
INE 146
141
MUX
31UNITS
92a
SN INPUT 99
REF INPUTS 130
CA INPUTS 131
Φ1
Φ2
91a
91b
MUX
MUX
31UNITS
92b
31UNITS
92c
Φ1
AGND 54
Φ2
91b
93b
Φ2g
Φ1g
93a
AGND 54
94
Φ1az
16 UNITS
92d
95
osz
16 UNITS
92c
Φ2en
Φ1en
96b
96a
AGND 54
+
-
Φ2
91b
OUT 98
OS
97
OBUS 25

FIGURE 11

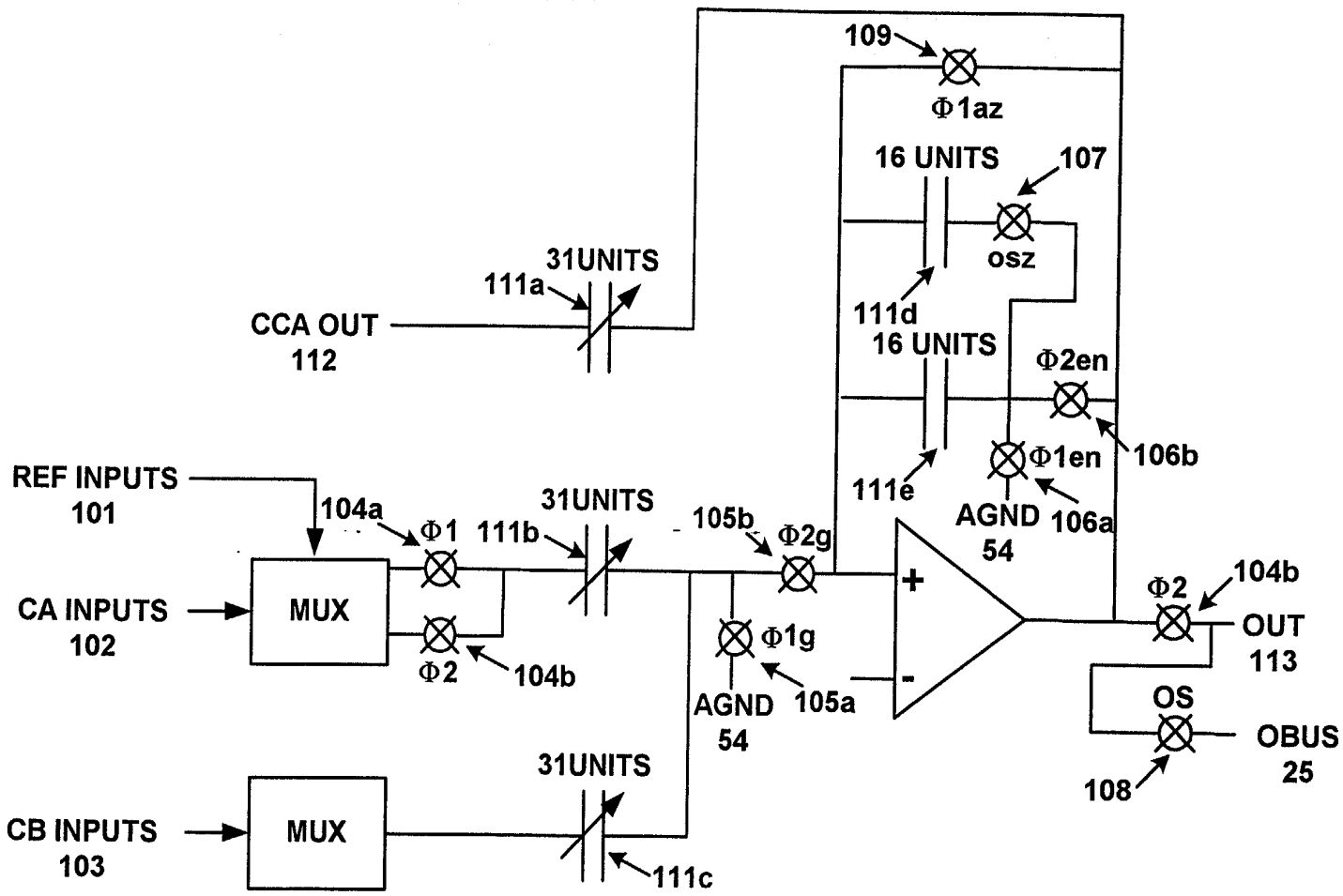
100
109
Φ1az
16 UNITS
107
osz
31UNITS
111a
CCA OUT
112
111d
16 UNITS
Φ2en
Φ1en
106b
111e
AGND
54
106a
REF INPUTS
101
104a
Φ1
111b
31UNITS
105b
Φ2g
CA INPUTS
102
MUX
Φ2
104b
Φ1g
AGND
54
105a
+
-
Φ2
104b
OUT
113
OS
OBUS
25
108
31UNITS
CB INPUTS
103
MUX
111c

FIGURE 12A

100a

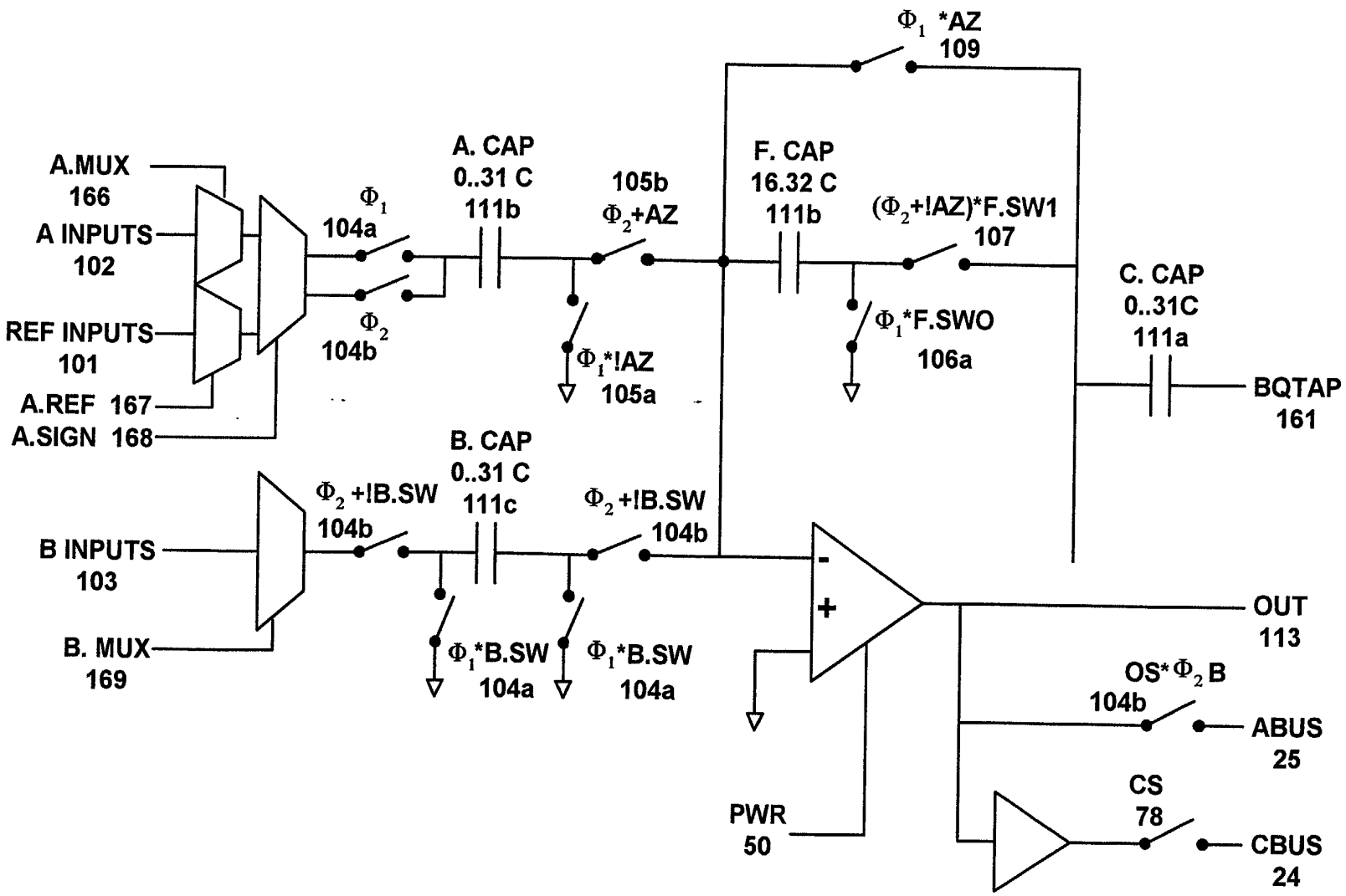

FIGURE 12B

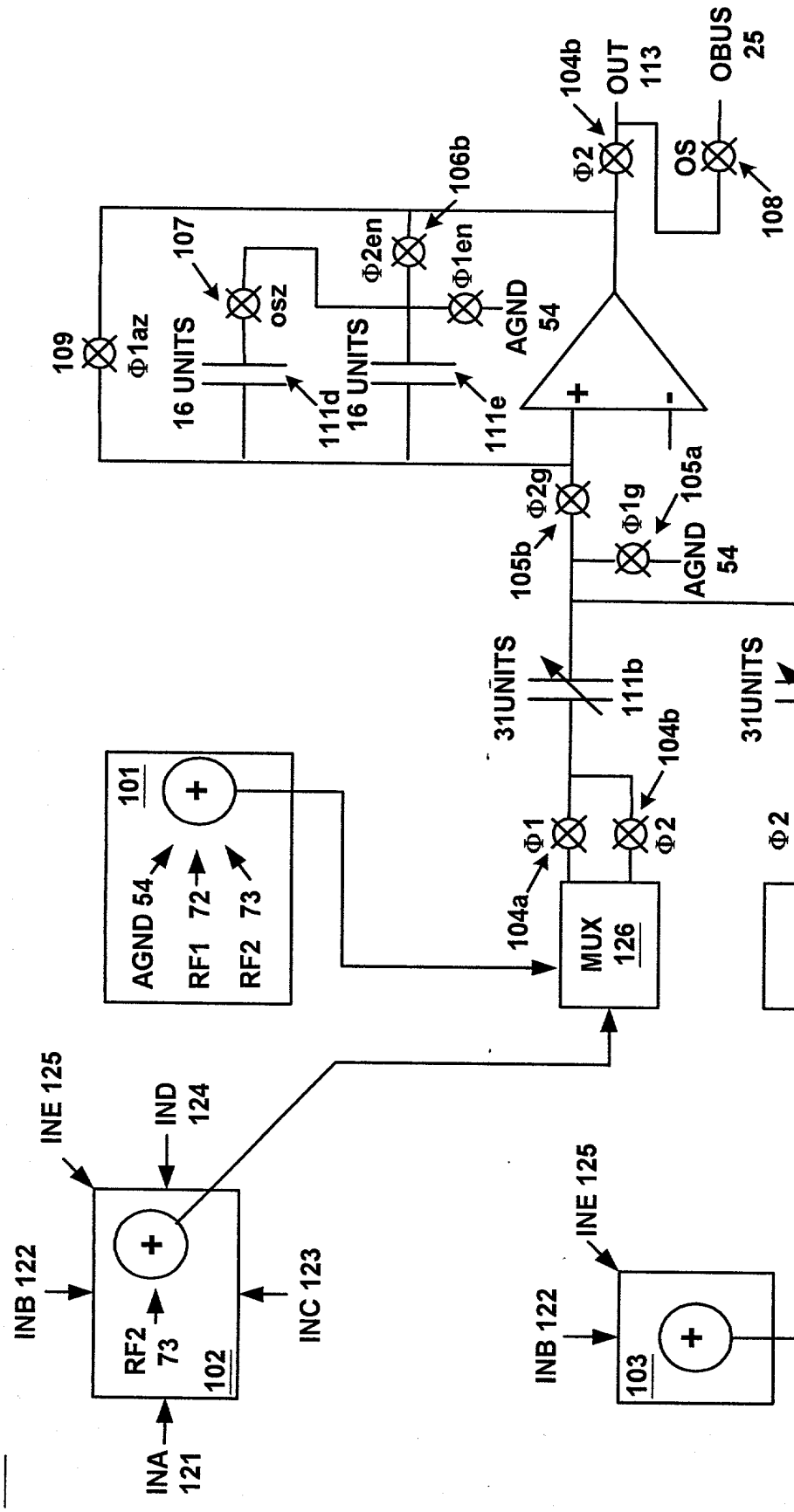
100
INA 121
INB 122
INC 123
INE 125
IND 124
RF2 73
102
AGND 54
RF1 72
RF2 73
101
INE 125
INB 122
103
MUX 126
104a
Φ1
Φ2
104b
31UNITS
111b
MUX
Φ2
104b
31UNITS
111c
Φ1
104a
AGND 54
105b
Φ2g
Φ1g
105a
AGND 54
109
Φ1az
16 UNITS
111d
107
osz
16 UNITS
111e
Φ2en
Φ1en
106b
AGND 54
+
-
Φ2
104b
OUT 113
OS
108
OBUS 25

FIGURE 13

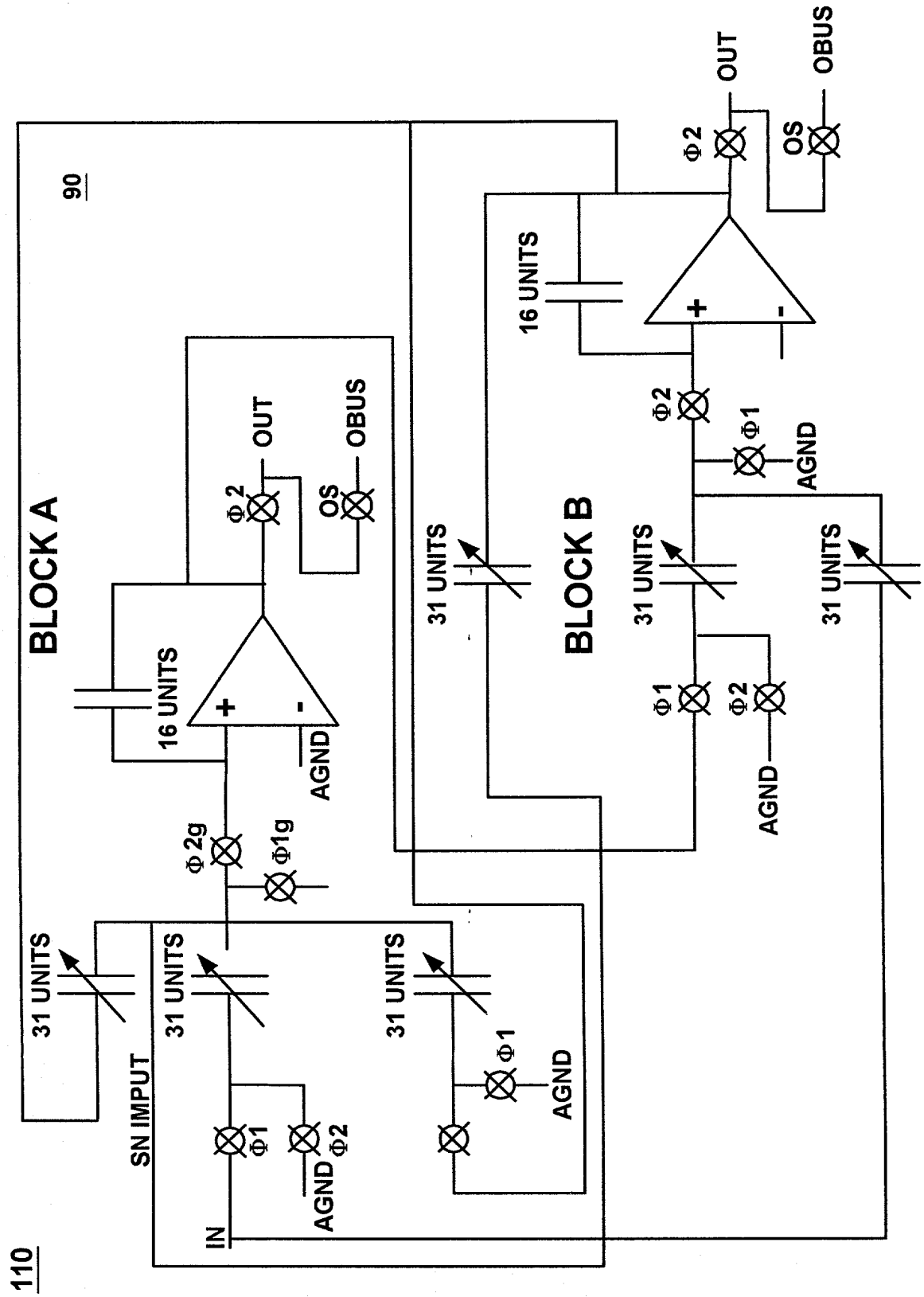
110
90
BLOCK A
BLOCK B
SN IMPUT
IN
31 UNITS
16 UNITS
Φ1
Φ2
Φ1g
Φ2g
AGND
OUT
OBUS
OS
+
-

FIGURE 14A

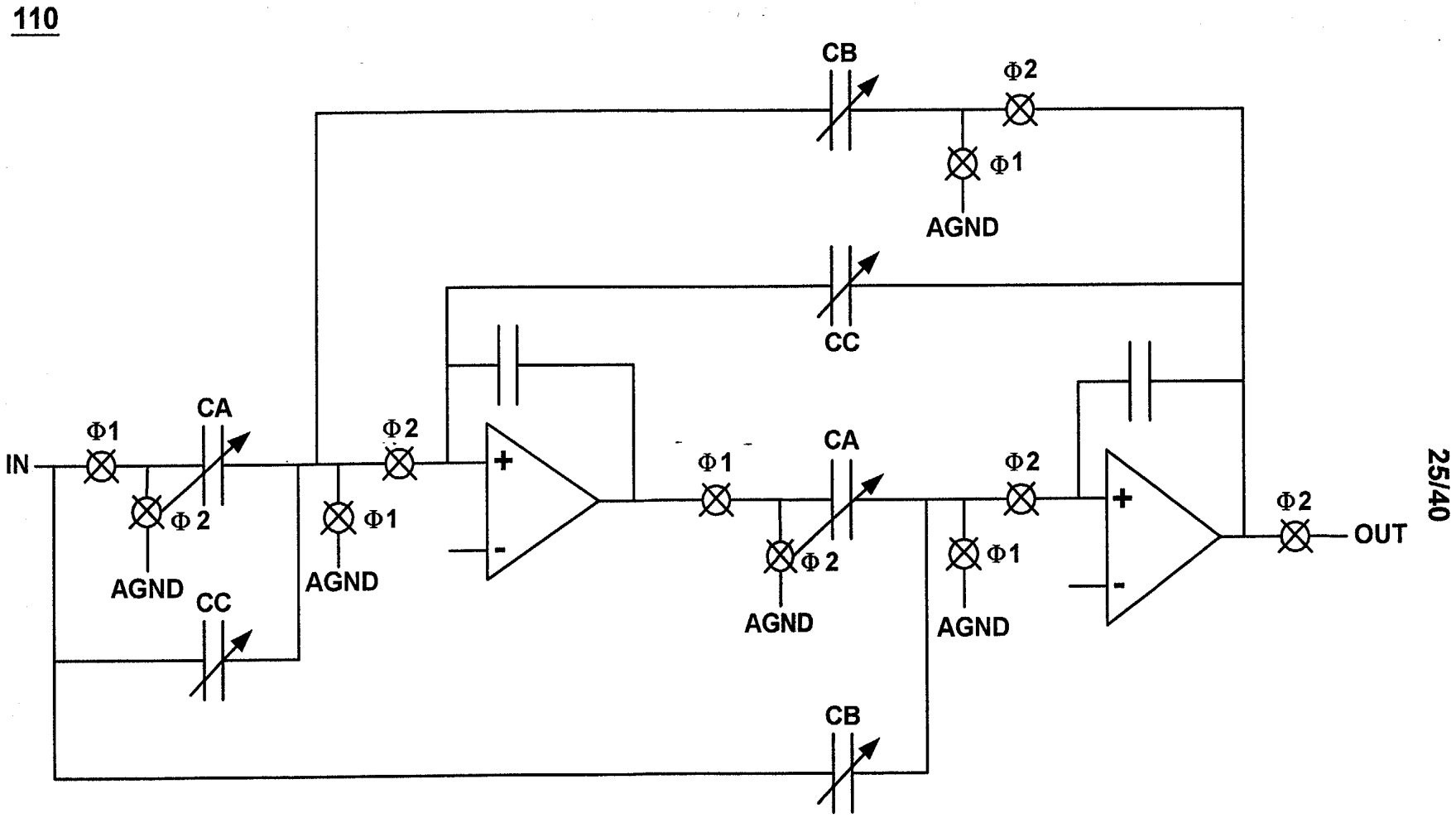
110
CB
Φ2
Φ1
AGND
CC
IN
Φ1
CA
Φ2
AGND
Φ2
Φ1
AGND
CC
Φ1
CA
Φ2
AGND
Φ2
Φ1
AGND
Φ2
OUT
CB

FIGURE 14B

1500

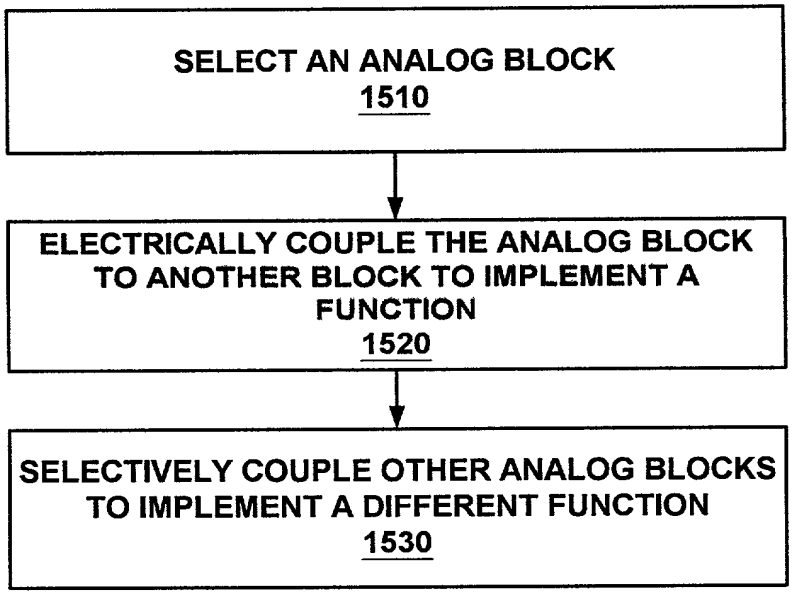

FIGURE 15

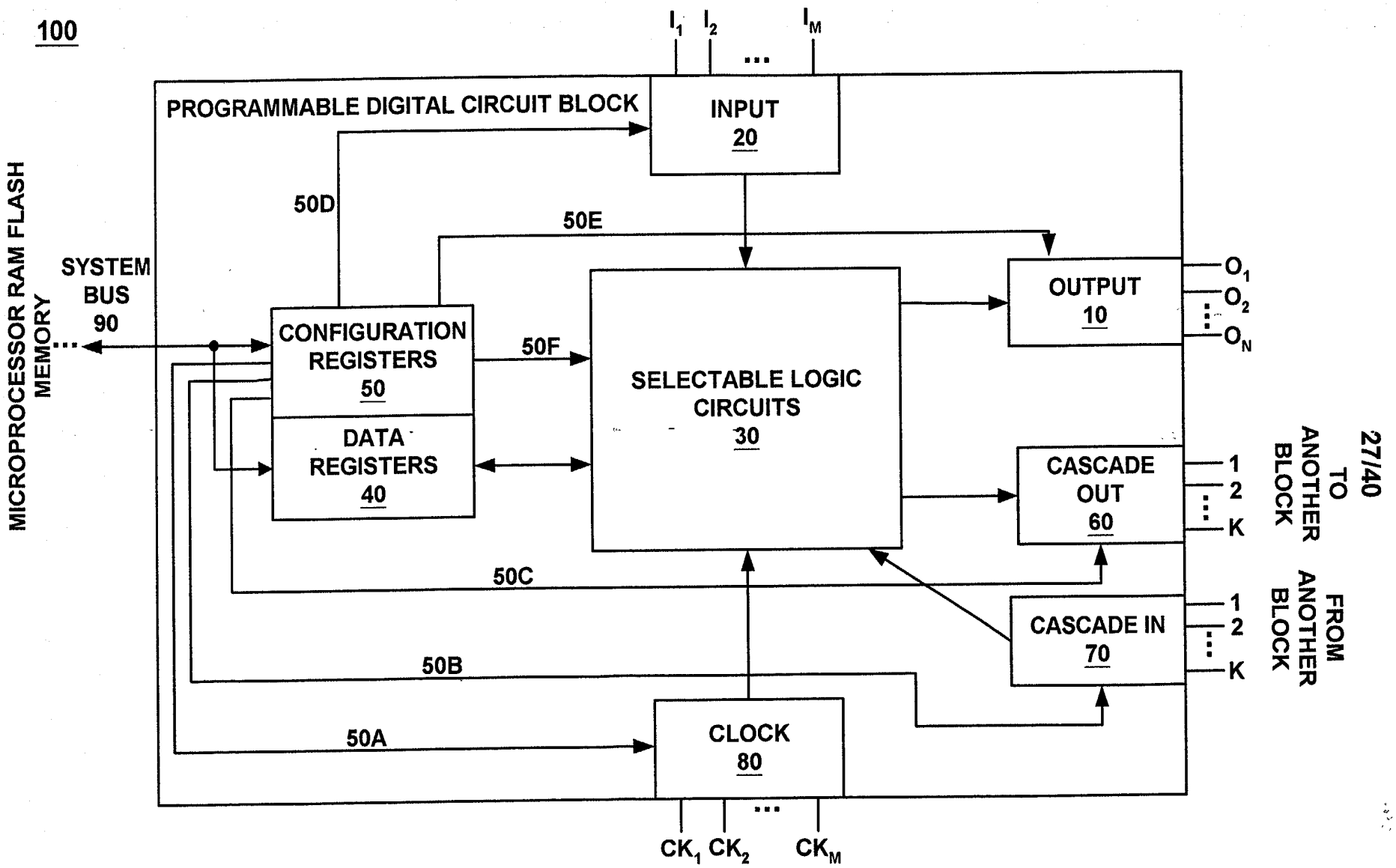
100
I_1 I_2 ... I_M
PROGRAMMABLE DIGITAL CIRCUIT BLOCK
INPUT
20
50D
50E
SYSTEM
BUS
90
MICROPROCESSOR RAM FLASH MEMORY
CONFIGURATION
REGISTERS
50
50F
DATA
REGISTERS
40
SELECTABLE LOGIC
CIRCUITS
30
OUTPUT
10
O_1
O_2
O_N
CASCADE
OUT
60
1
2
K
50C
CASCADE IN
70
1
2
K
FROM ANOTHER BLOCK
TO ANOTHER BLOCK
27/40
50B
50A
CLOCK
80
CK_1 CK_2 ... CK_M

FIGURE 16

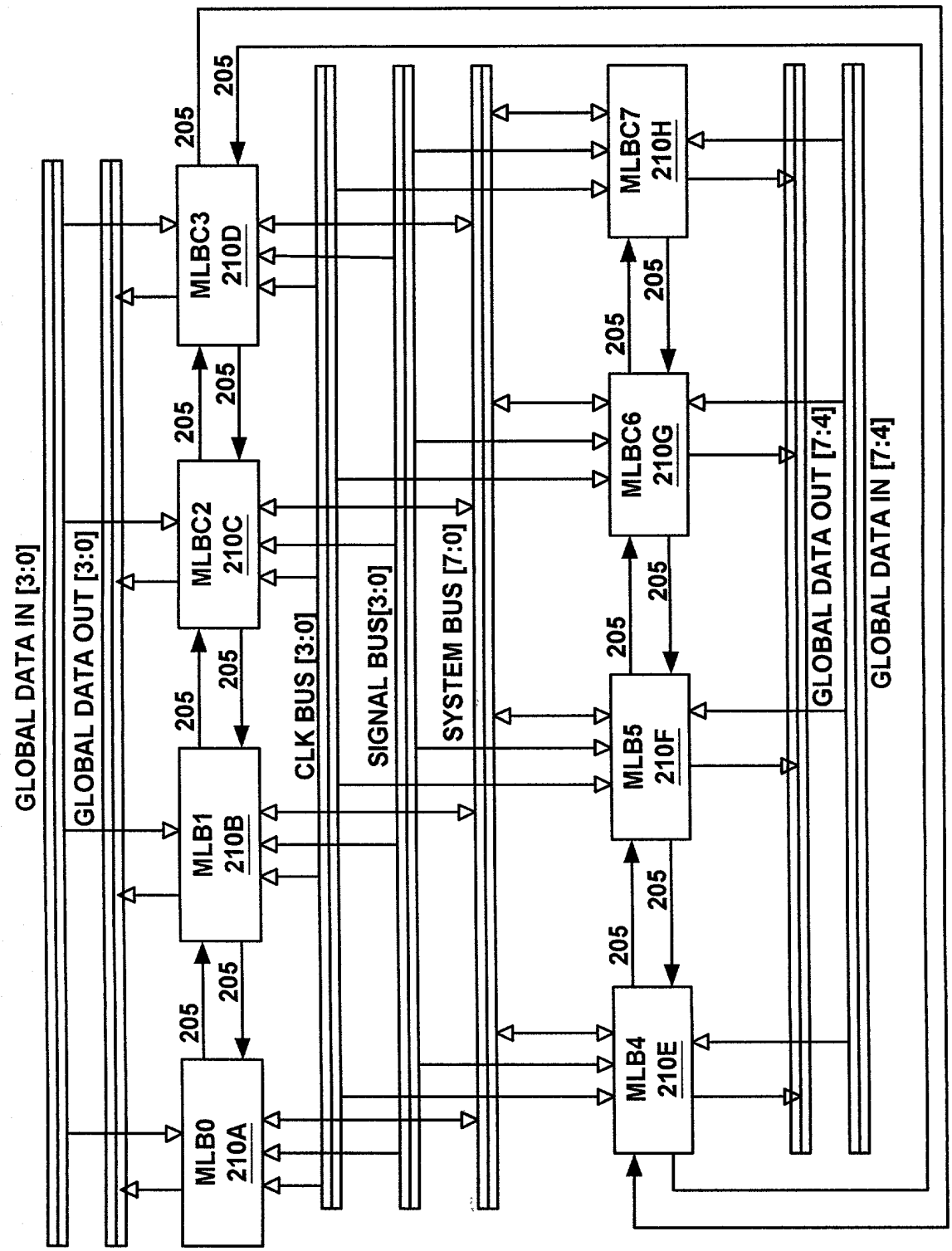
200
GLOBAL DATA IN [3:0]
GLOBAL DATA OUT [3:0]
CLK BUS [3:0]
SIGNAL BUS[3:0]
SYSTEM BUS [7:0]
GLOBAL DATA OUT [7:4]
GLOBAL DATA IN [7:4]
MLB0 210A
MLB1 210B
MLBC2 210C
MLBC3 210D
MLB4 210E
MLB5 210F
MLBC6 210G
MLBC7 210H
205

FIGURE 17

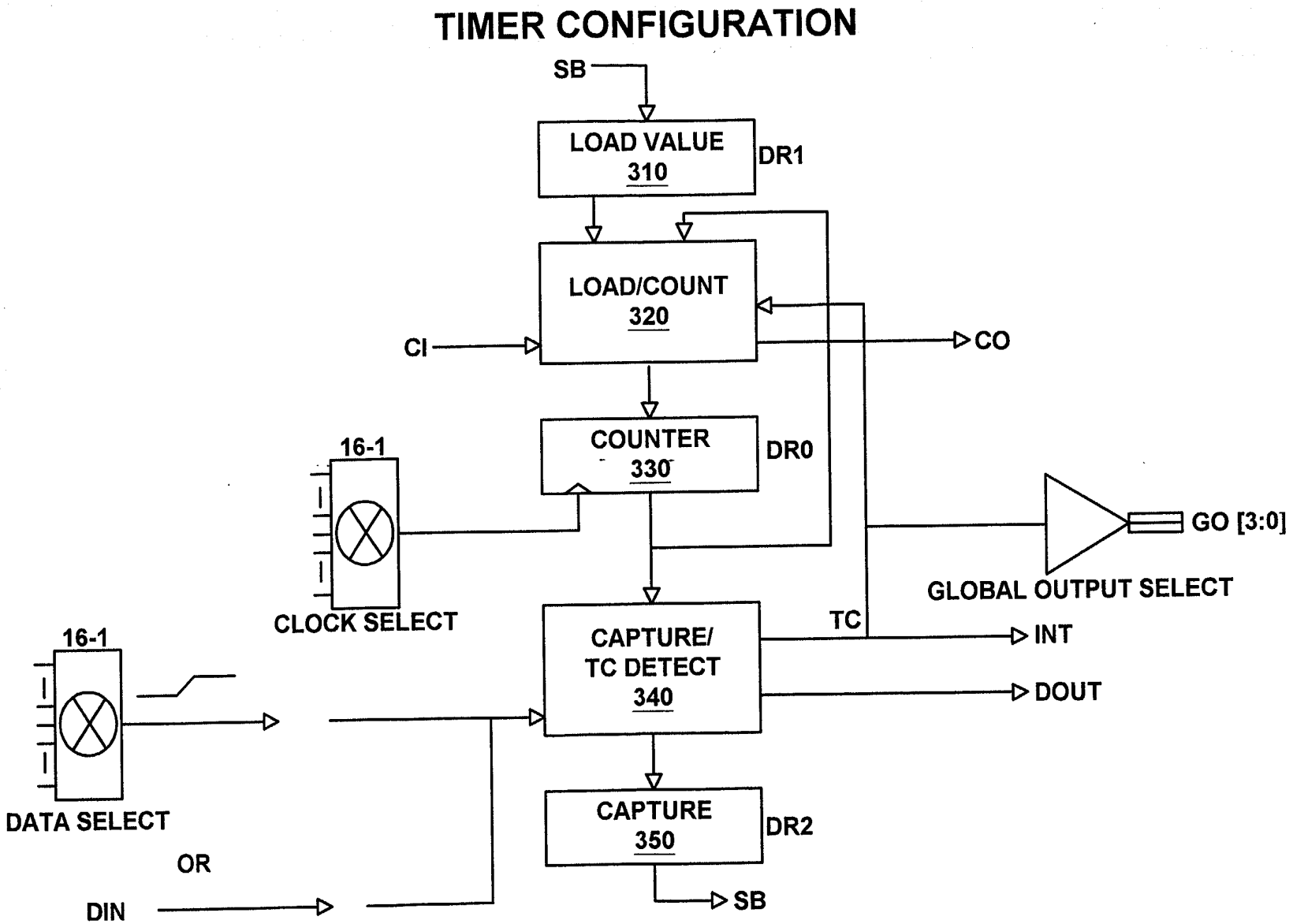

FIGURE 18

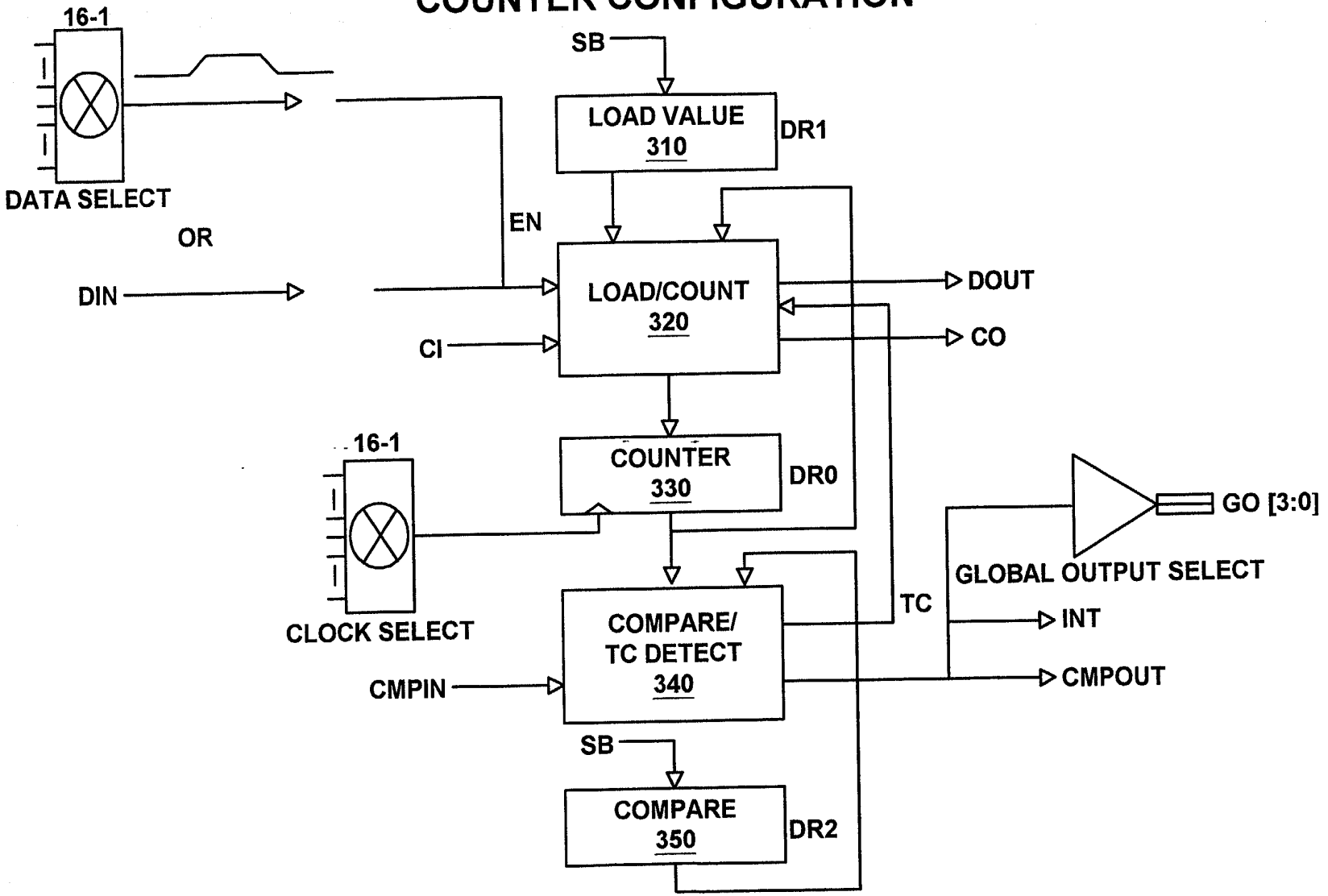
COUNTER CONFIGURATION
16-1
DATA SELECT
OR
DIN
SB
LOAD VALUE
310
DR1
EN
LOAD/COUNT
320
DOUT
CO
CI
16-1
COUNTER
330
DR0
CLOCK SELECT
GO [3:0]
GLOBAL OUTPUT SELECT
TC
INT
CMPOUT
COMPARE/
TC DETECT
340
CMPIN
SB
COMPARE
350
DR2

FIGURE 19

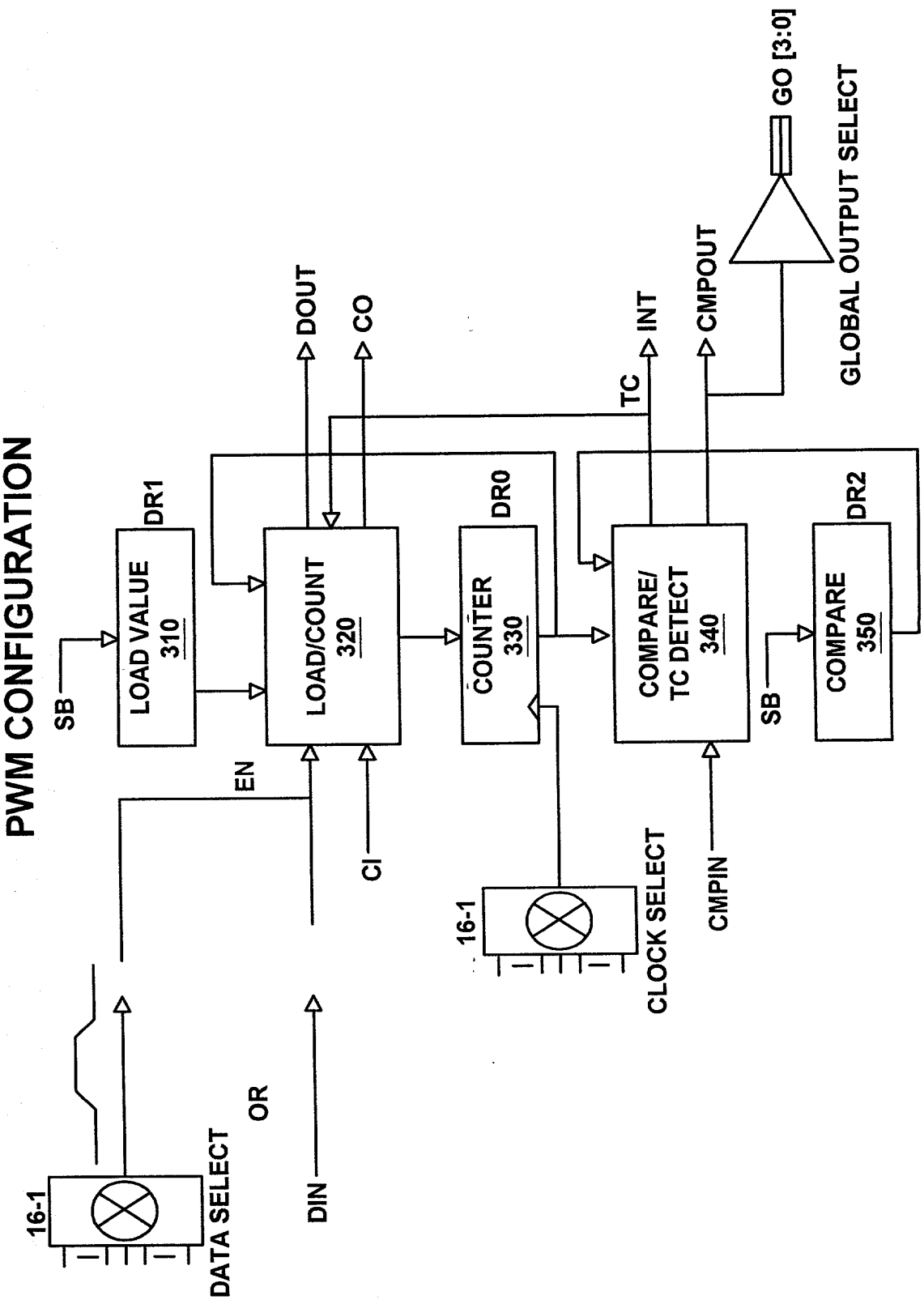
PWM CONFIGURATION
SB
LOAD VALUE 310
DR1
LOAD/COUNT 320
DOUT
CO
EN
CI
DIN
OR
16-1
DATA SELECT
COUNTER 330
DR0
16-1
CLOCK SELECT
COMPARE/ TC DETECT 340
TC
INT
CMPOUT
CMPIN
SB
COMPARE 350
DR2
GO [3:0]
GLOBAL OUTPUT SELECT

FIGURE 20

TX UART CONFIGURATION

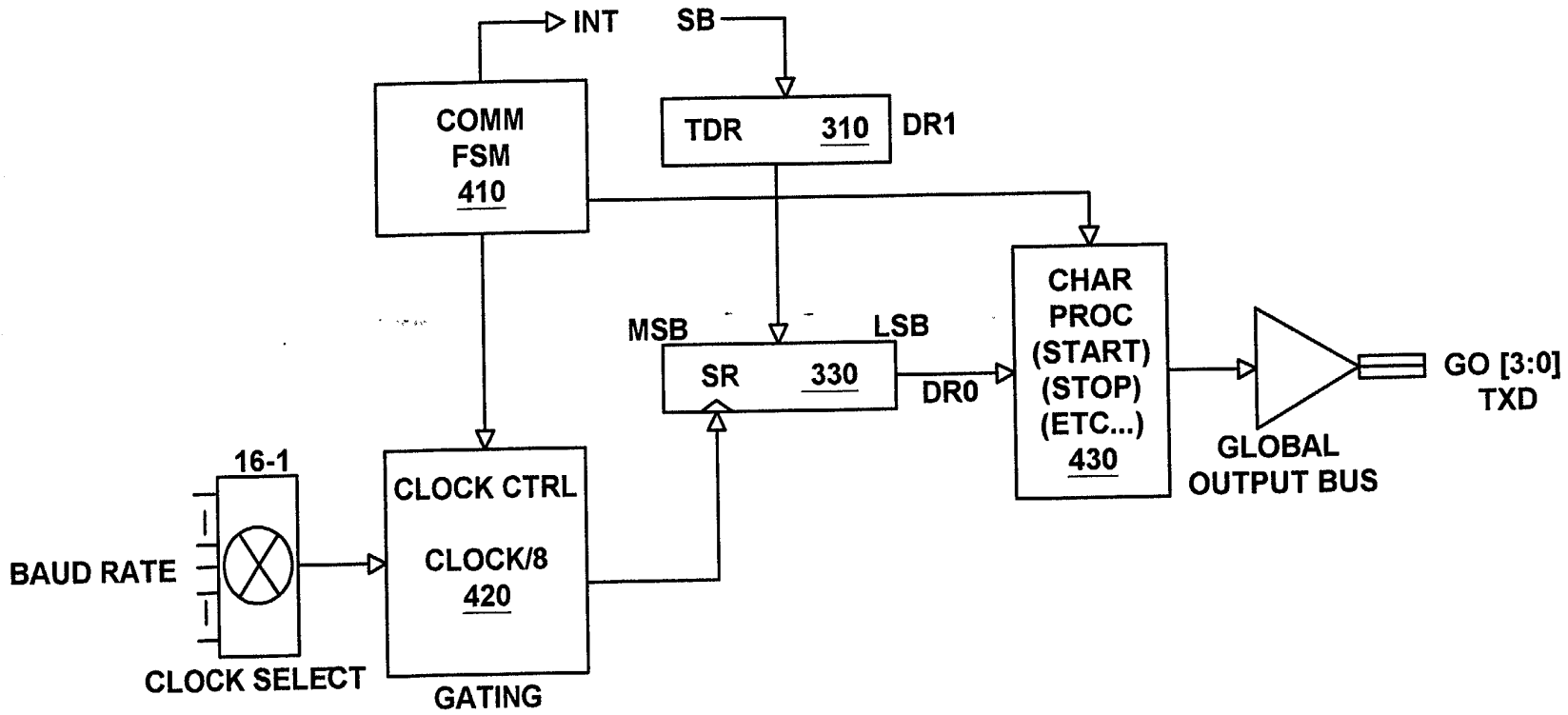

FIGURE 21

RX UART CONFIGURATION

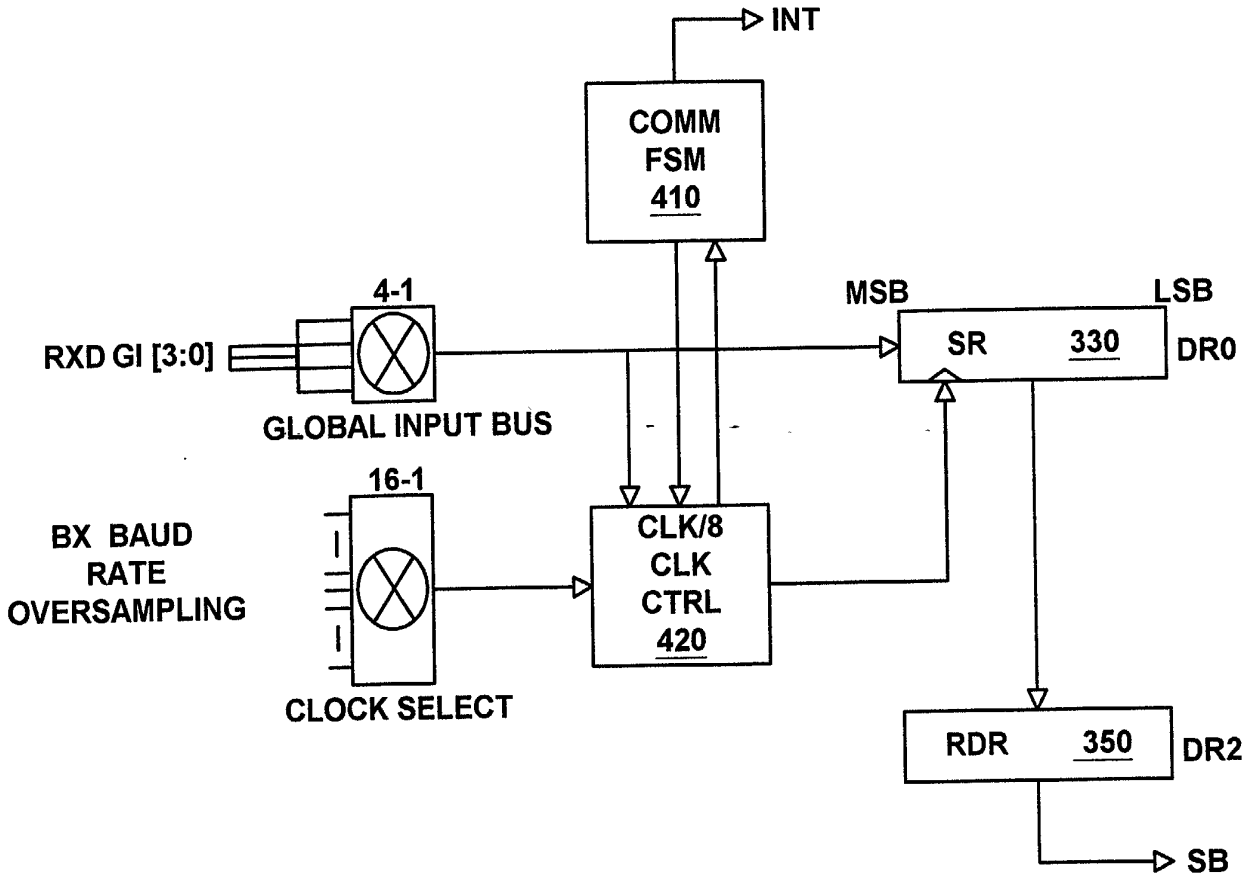

FIGURE 22

SPI MASTER CONFIGURATION

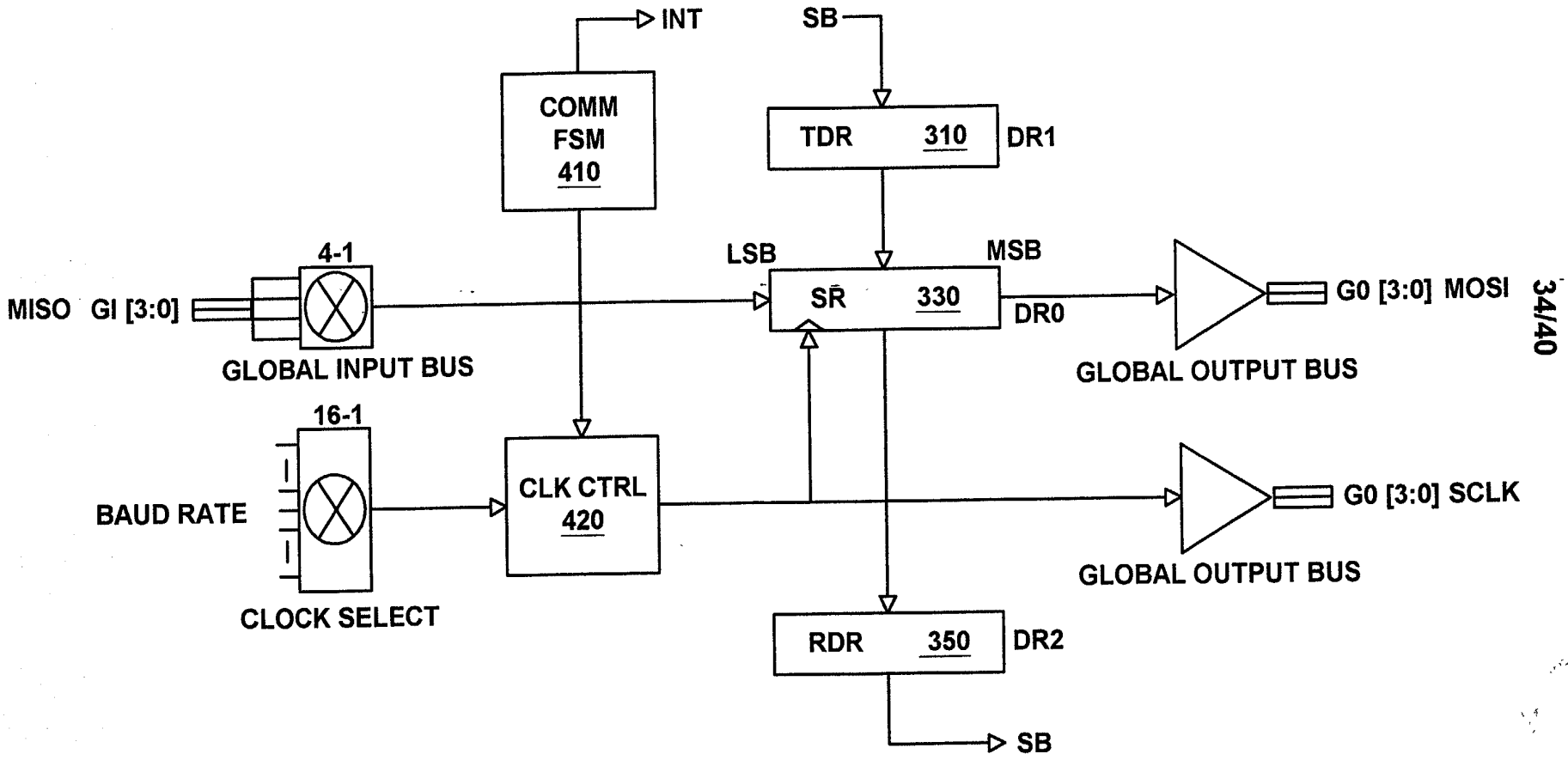

FIGURE 23

SPI SLAVE CONFIGURATION

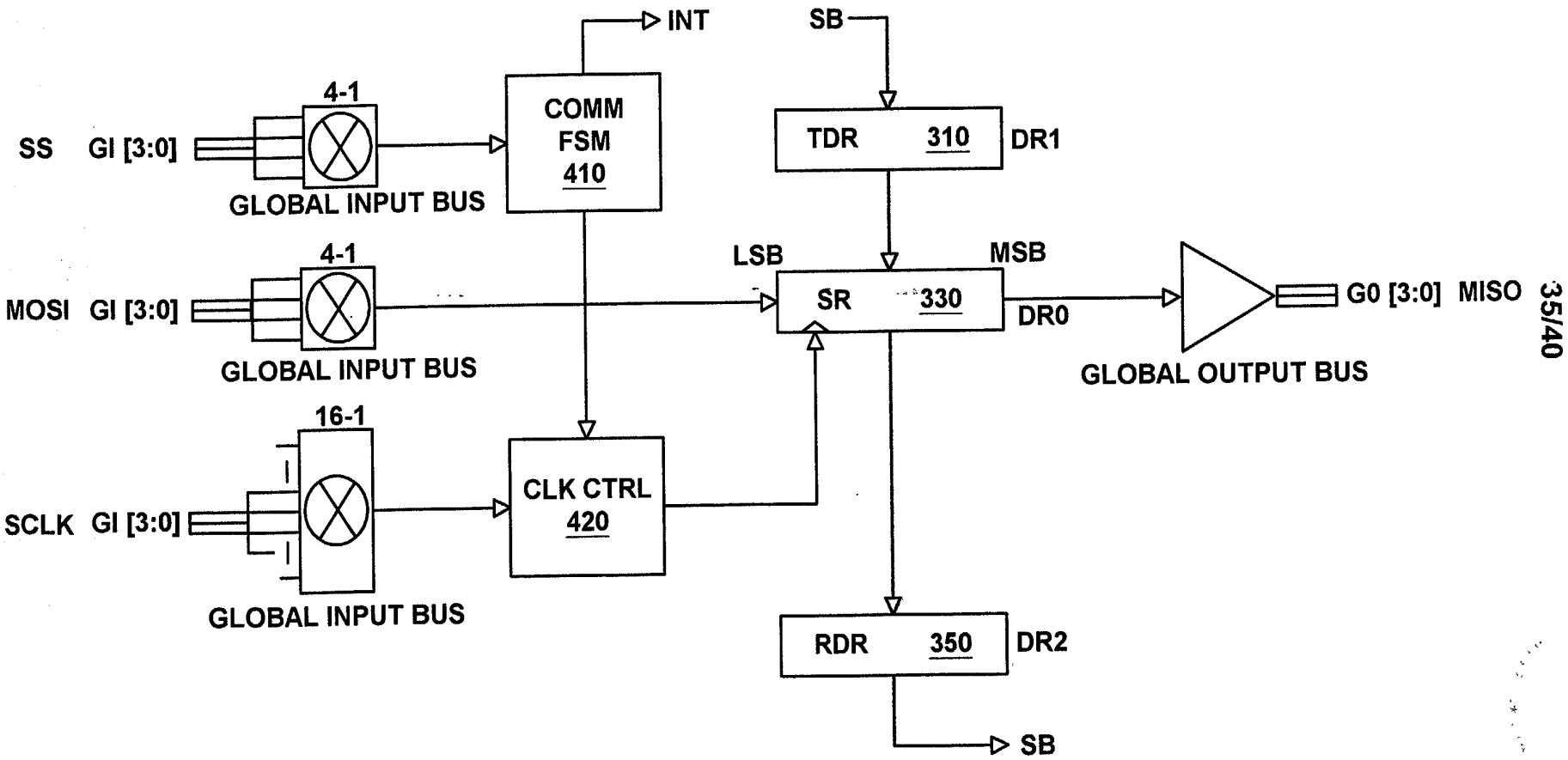

FIGURE 24

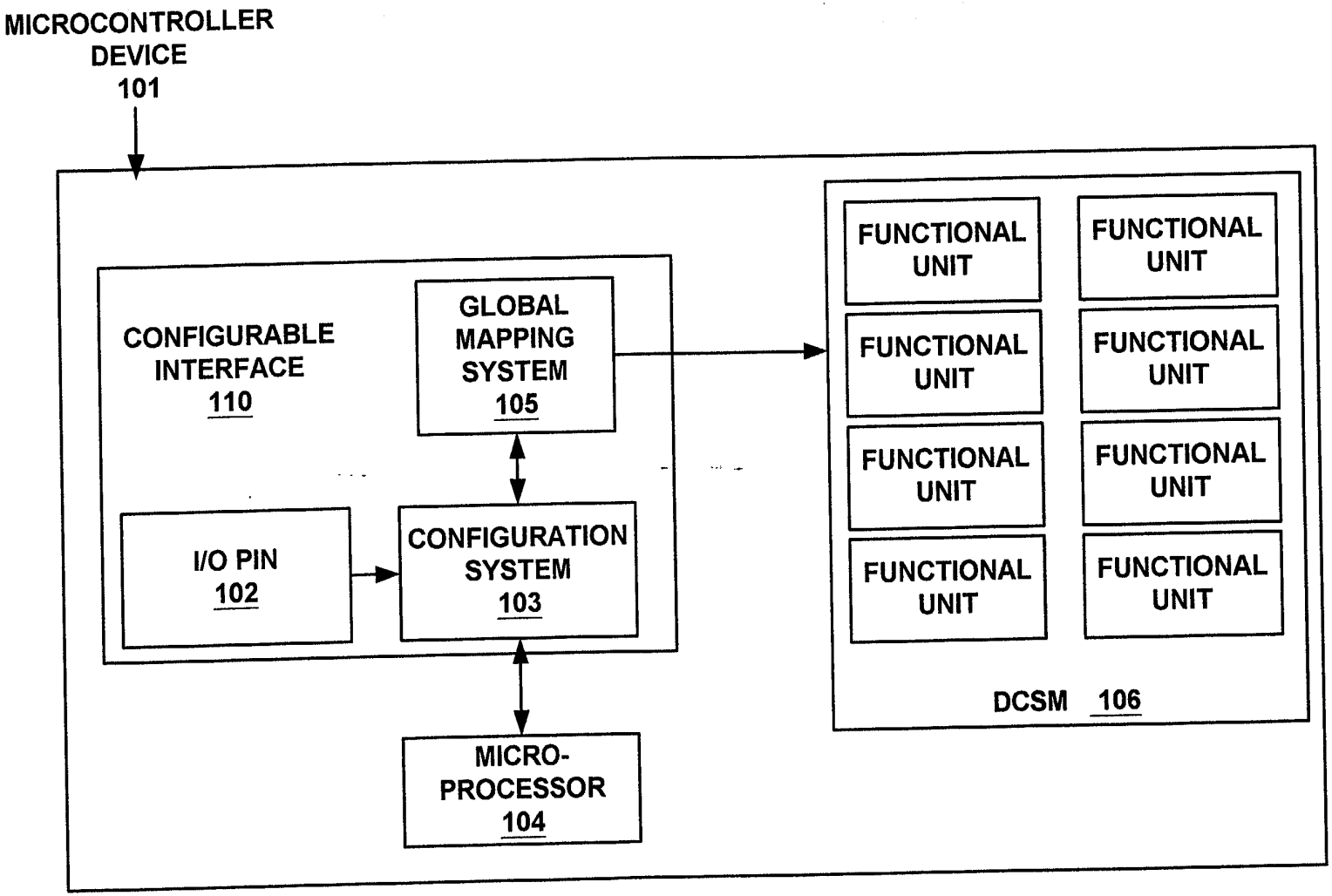
MICROCONTROLLER
DEVICE
101
CONFIGURABLE
INTERFACE
110
GLOBAL
MAPPING
SYSTEM
105
I/O PIN
102
CONFIGURATION
SYSTEM
103
MICRO-
PROCESSOR
104
FUNCTIONAL
UNIT
FUNCTIONAL
UNIT
FUNCTIONAL
UNIT
FUNCTIONAL
UNIT
FUNCTIONAL
UNIT
FUNCTIONAL
UNIT
FUNCTIONAL
UNIT
FUNCTIONAL
UNIT
DCSM 106

FIGURE 25

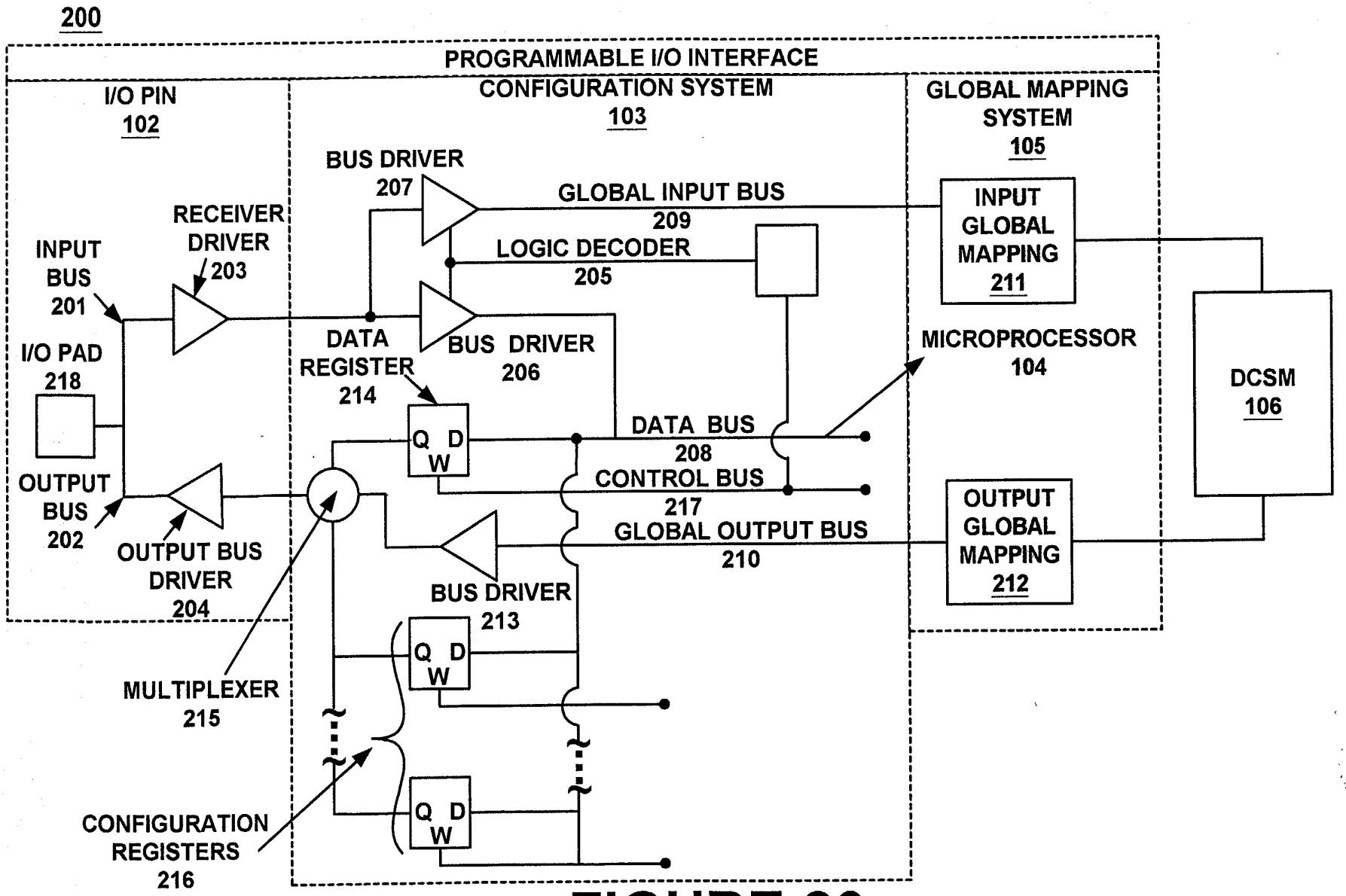
200
PROGRAMMABLE I/O INTERFACE
I/O PIN
102
CONFIGURATION SYSTEM
103
GLOBAL MAPPING
SYSTEM
105
BUS DRIVER
207
GLOBAL INPUT BUS
209
INPUT
GLOBAL
MAPPING
211
RECEIVER
DRIVER
203
INPUT
BUS
201
LOGIC DECODER
205
I/O PAD
218
DATA
REGISTER
214
BUS DRIVER
206
MICROPROCESSOR
104
DCSM
106
Q D
W
DATA BUS
208
CONTROL BUS
217
OUTPUT
BUS
202
OUTPUT BUS
DRIVER
204
GLOBAL OUTPUT BUS
210
OUTPUT
GLOBAL
MAPPING
212
BUS DRIVER
213
MULTIPLEXER
215
CONFIGURATION
REGISTERS
216

FIGURE 26

300

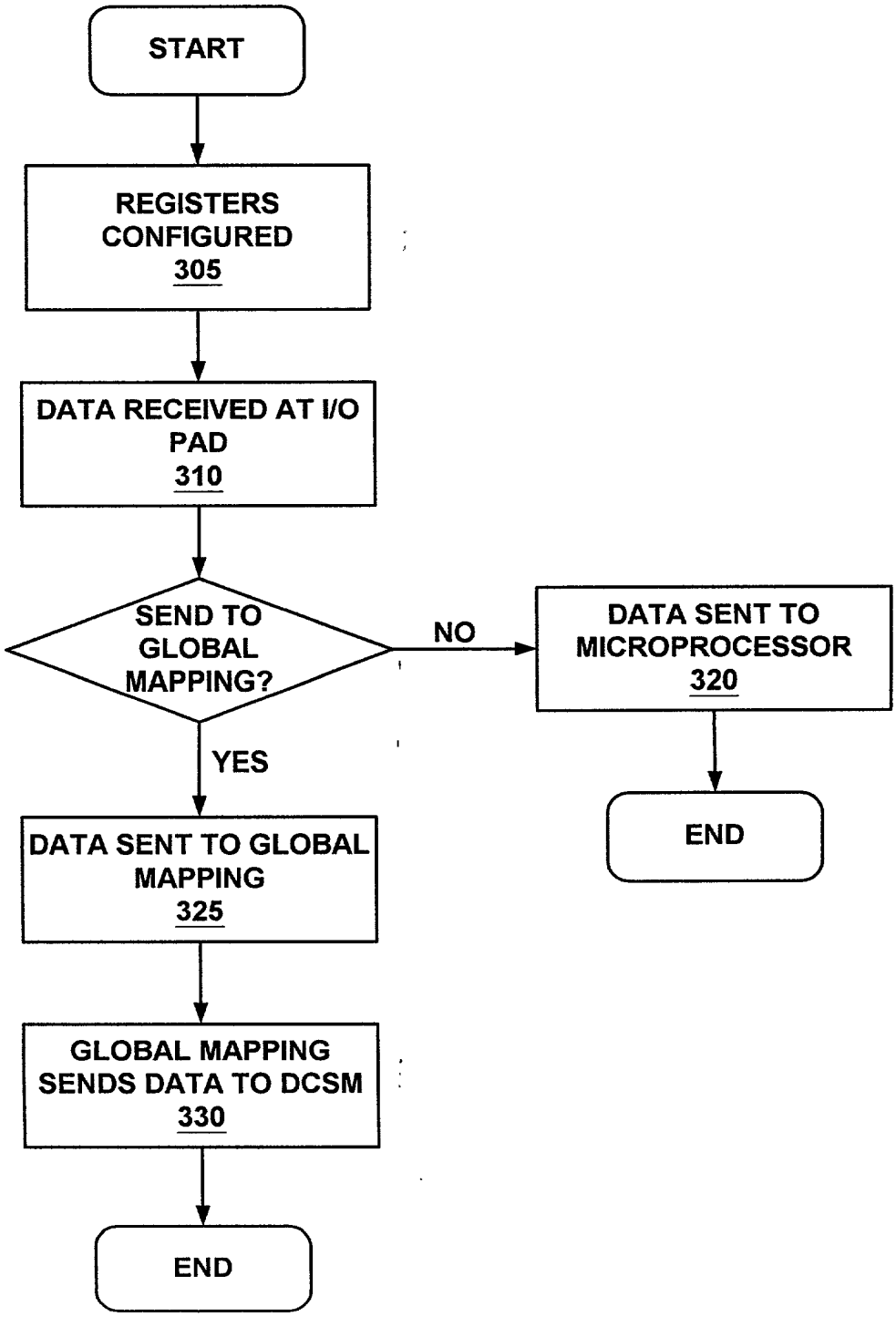

FIGURE 27

400

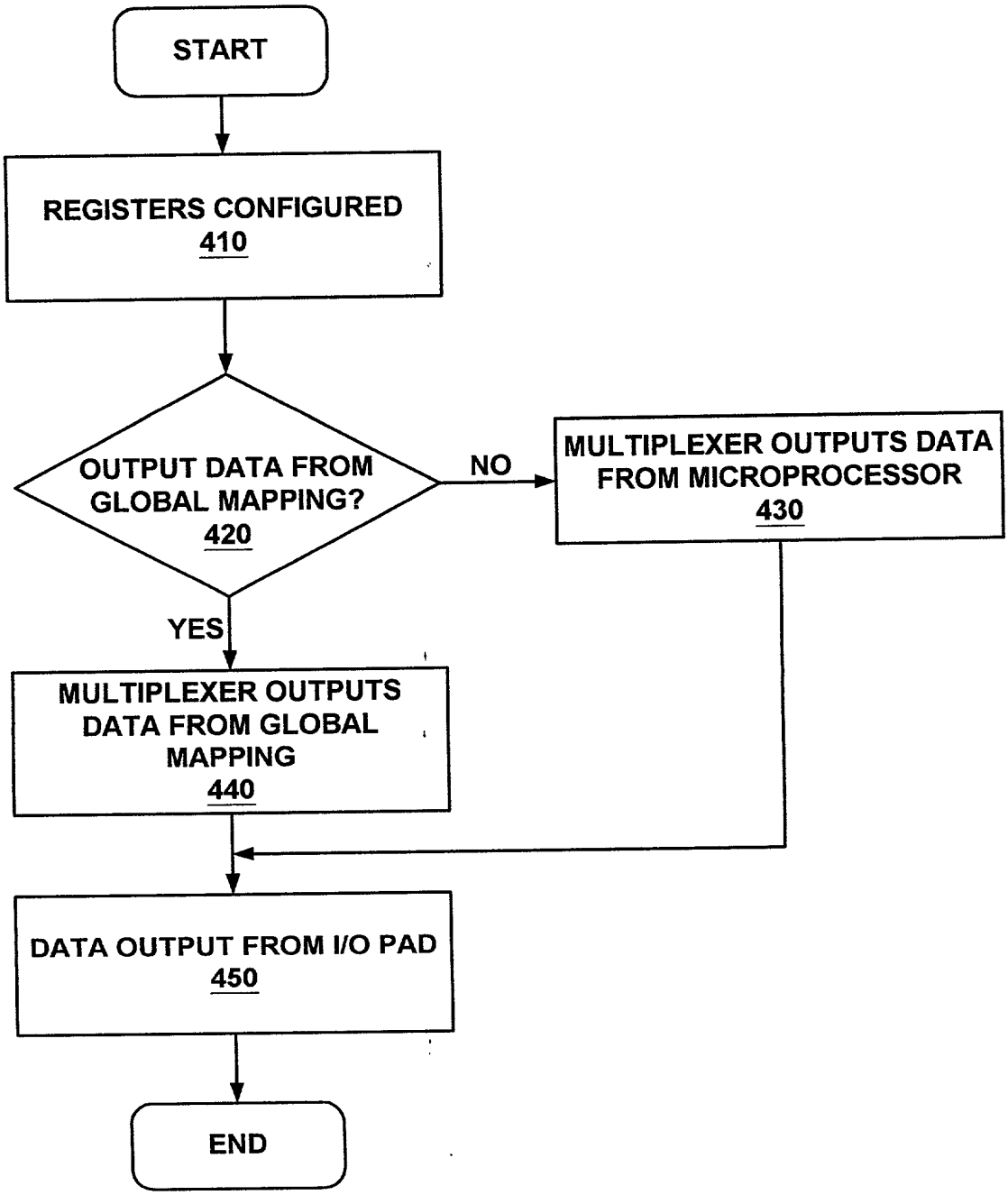

FIGURE 28

2900

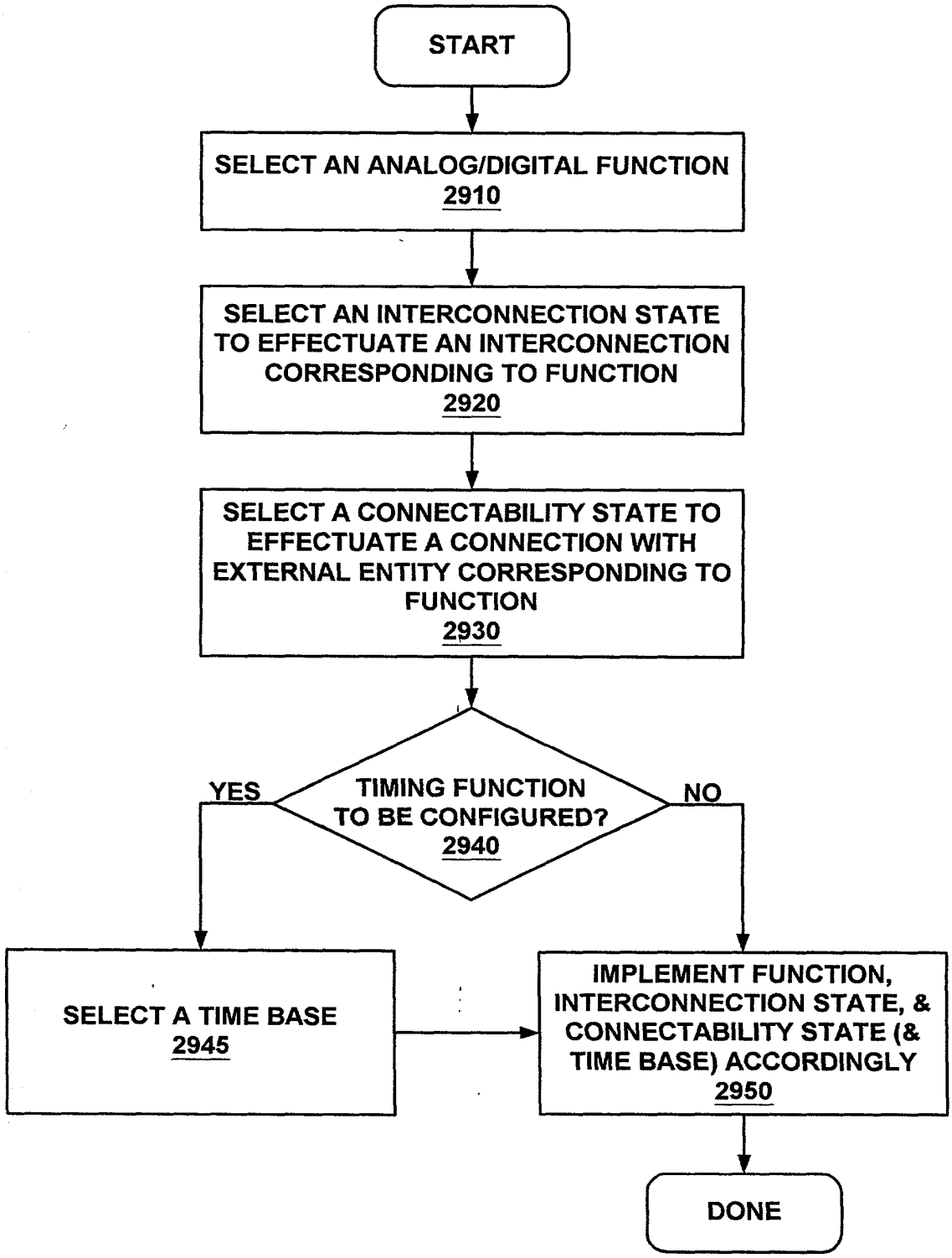

FIGURE 29